ME-902

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HANDBOOK OF INSTRUCTIONS FOR MEC MODEL 72 DATA RECEIVER

prepared for
National Aeronautics and Space Administration
Contract No. NAS 1-430

30 November 1960

Revised 25 September, 1961

Milgo Electronic Corporation
for
International Business Machines Corporation

in association with

WESTERN ELECTRIC COMPANY, INC.

LIST OF EFFECTIVE PAGES

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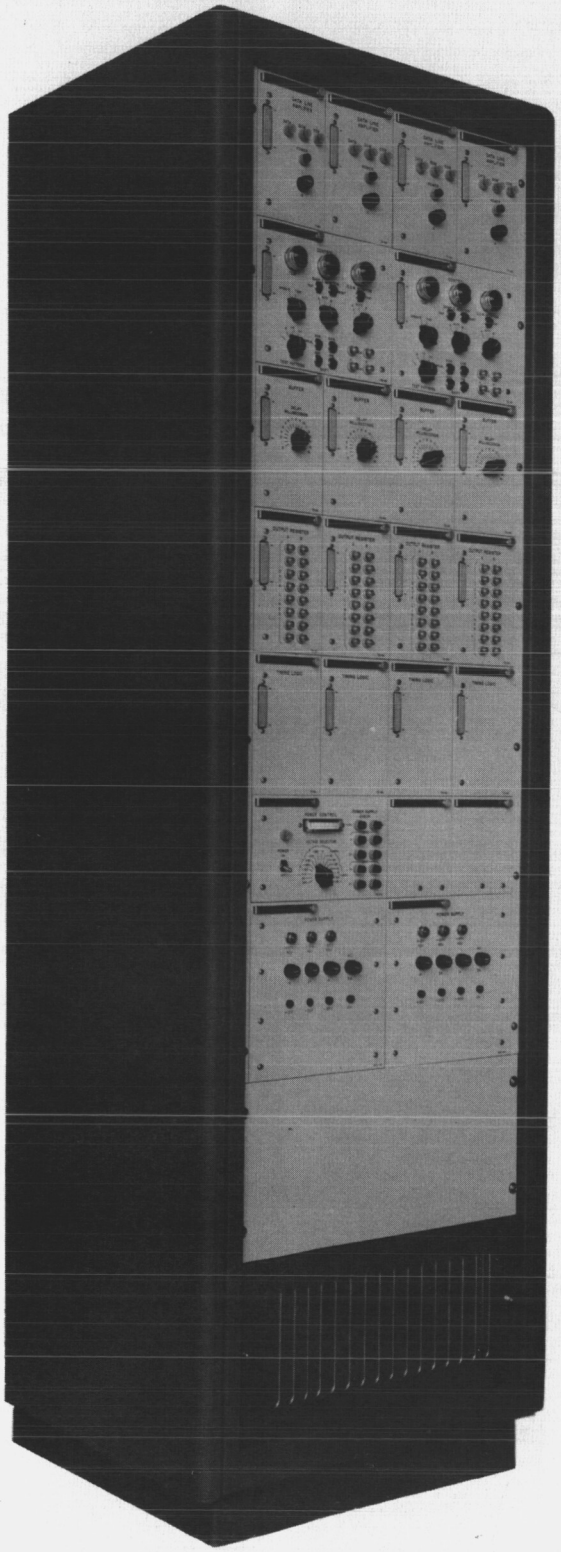


Figure 1-1. MEC Model 72 Data Receiver

CHAPTER I

INTRODUCTION

1-1. PURPOSE OF EQUIPMENT (Figure 1-1)

1-1.1. The MEC Model 72 Data Receiver accepts four channels of data which have been transmitted over telephone voice lines in two pairs, with time displacement, by MEC Models 70 and 71 Data Transmitters. Misalignment of the data is done in order to lessen the possibility of external noise affecting all data channels in a like fashion once it leaves the source. The Receiver aligns the time displaced data and supplies it to two IBM Data Communication Channels (DCC), formerly referred to as Real Time Channels (RTC).

1-1.2. The only restriction placed upon the data format by the Receiver is the requirement of Start of Word (SOW) and End of Word (EOW) respectively, before and after each message. The length of the message is limited only by the equipment receiving the data from the Receiver, provided the data consists of an integral number of 8 bits. The data enters the Receiver in serial form, is aligned and converted into parallel groups of 8 bits, and is sent out in a form complying with the input levels required by the DCC.

1-2. SCOPE OF MANUAL

This instruction manual describes the MEC (Milgo Electronic Corporation) Model 72 Data Receiver, designed and manufactured by Milgo Electronic Corporation, for International Business Machines, Federal Systems Division, Kingston, New York, in conjunction with Project Mercury.

1-3. PURPOSE OF MANUAL

1-3.1. This instruction manual is provided as an aid to better understanding the operation, and theory behind the MEC Model 72 Data Receiver, and its associated equipment. It offers a complete technical explanation coupled with applicable illustrations, with an estimation of the interest and questions of the qualified technician.

1-3.2. It is strongly urged that the operator, or any person involved in the operation of this equipment, thoroughly read and fully understand the contents of this manual.

CHAPTER II
GENERAL DESCRIPTION

2-1. GENERAL

2-1.1. The MEC Model 72 Data Receiver receives data with a time displacement of not more than 16 milliseconds. It aligns this data internally before sending it to the DCC. The outputs of the Receiver consist of 8 lines to each DCC, divided into four pairs (one pair per Output Register): a sample line, an EOW line, and a ground reference to each of the two subchannels of each DCC.

2-1.2. The Data Receiver contains four individual receivers combined into two "receiver pairs" operating independently. Each receiver pair receives and aligns two channels of data which originate from a single source, one channel having been time displaced with respect to the other.

2-2. PHYSICAL DESCRIPTION (Figure 2-1)

The Model 72 Data Receiver is housed in a standard rack approximately 74-1/8 inches high, 24 inches wide, and 22 inches deep. Its weight is approximately 660 pounds. All chassis are of modular construction and employ 50 pin connectors to effect the connection of each chassis to rack wiring. All chassis of a particular type are interchangeable, and they are keyed, making it impossible for insertion into an incorrect rack position. Rack chassis are locked in place by a single screw type locking handle.

2-3. INPUTS

The Data Receiver accepts modulated tone bursts of approximately 2 kc at a 1 kc repetition rate from voice channels on balanced or unbalanced 600 ohm communication lines, equalized for a 1 kc data bit rate. Data consists of 0.5 millisecond bursts; SOW a 2.5 millisecond burst; and EOW, a 4.5 millisecond burst. Input signal requirements are from -30 dbm to +10 dbm. Minimum signal to noise ratio is in the order of 3:1 in the band pass range. Outside this band pass range attenuation should be at least 20 db per octave.

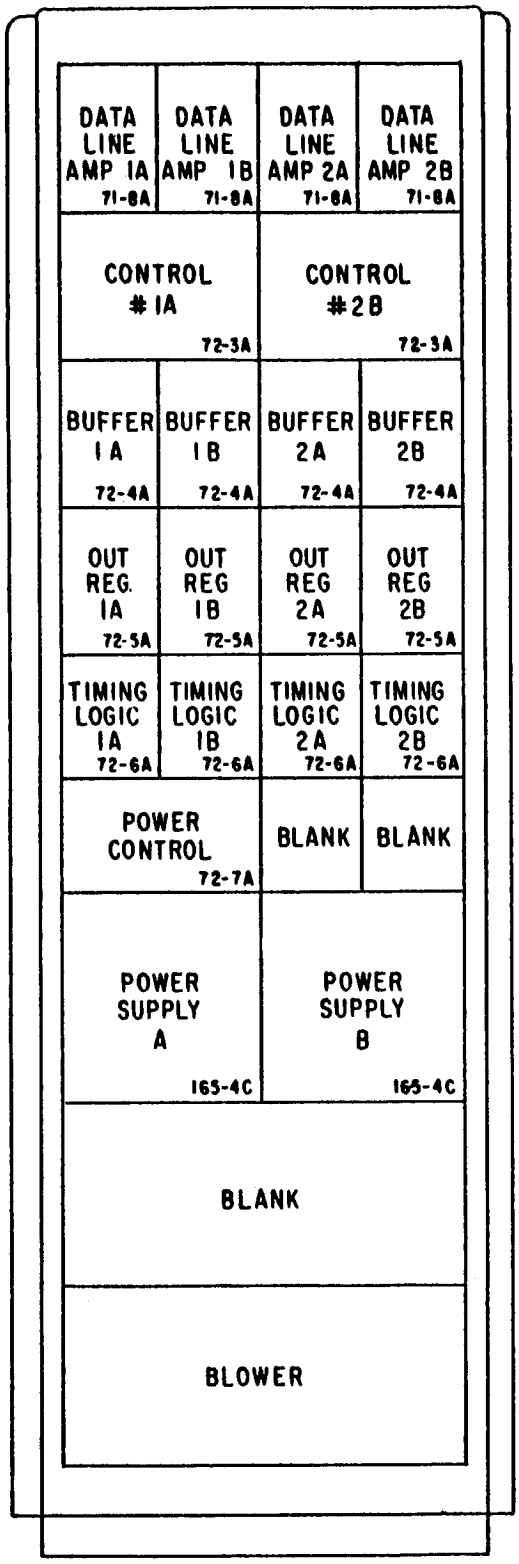


Figure 2-1. Chassis Arrangement

The Data Receiver requires 120 vac single phase at approximately 8 amperes as power inputs.

2-4. OUTPUTS

2-4.1. Each of the four Output Registers has eight data outputs connected to each DCC for a total of 64 data line outputs. Each Control Chassis has a sample and EOW line to each subchannel of a DCC. Therefore, the total number of outputs is 64 data lines, 4 sample lines, and 4 EOW lines. There are also provisions for signal ground reference to each DCC subchannel.

2-4.2. When the Buffer Chassis have been properly set, via switch S401 on the front panel, all data should appear at the outputs of a given pair of Output Registers within one millisecond of each other. The associated sample pulse should occur approximately 5.5 milliseconds later. If EOW occurs, it will do so between the data and sample pulse.

2-4.3. Input signals to the DCC are as follows:

A binary 1 is 0 volts ±0.5 volts

A binary 0 is -10 volts nominal or from -6 to -12 volts.

Data and EOW outputs are levels. Sample pulse is a 10 microsecond pulse.

The outputs are tabulated in the lower left hand corner of Figure 9-10 showing the correlation of Receiver outputs to DCC inputs.

NOTE

Discussions concerning Power Supplies, Transistor Networks and Magnetic Cores will be found in the Appendix of this Manual.

CHAPTER III

THEORY OF OPERATION

3-1. GENERAL (Figure 9-1)

3-1.1. The Model 72 Data Receiver contains four individual receivers, and since they are used in groups of two to receive data from each of two sources, it is convenient to refer to the receivers as receiver pairs.

3-1.2. Data entering the Data Line Amplifier, #1A, proceeds to the Timing Logic #1A, Buffer #1A, Control A, and Output Register #1A before being shifted out to the DCC. These designations are shown in Figure 2-1. The companion data will follow suit in chassis numbered 1B, and the same is true of the remaining half of the rack. It is important to note that each half of a pair is wired from separate Power Supplies. Power Supply A supplies those chassis designated A and Power Supply B those designated B. Although each of the two receiver pairs receives data on two separate lines from a single source, the data on one of these lines may be delayed with respect to the other up to 16 milliseconds. This is done to insure that noise which disturbs data on one transmission line will not disturb the identical data being sent over another line. Each receiver pair is jointly powered by two Model 165-4C Power Supplies. The connection is such that failure of either Power Supply would only cause loss to half of a receiver pair, enabling the other half to operate satisfactorily.

3-1.3. Operate Mode - Data enters the Data Line Amplifiers in the form of 2 kc tone bursts. These tone bursts are separated into SOW pulses, data pulses, and EOW pulses. The output data line from the Data Line Amplifiers will contain pulses for both SOW and EOW, and the SOW line will have a pulse for EOW. As information is detected by the duration of a tone burst, EOW, for example, first resembles data, then SOW, before being recognized as EOW.

3-1.3.1. Assume a Data Line Amplifier has received a delayed EOW from a previous message. This action resets the 8:1 counter gate, flip-flop N606, in the Timing Logic Chassis, preparing it for a delayed SOW pulse. SOW is recognized by the Data Line Amplifier and inserted into the Buffer Chassis. Data follows the SOW pulse into the Buffer, the first bit following SOW by 2 milliseconds. SOW leaves the Buffer Chassis within 500 microseconds to 17.5 milliseconds after it enters, depending on the preset buffer delay. Delayed SOW sets the 8:1

counter gate allowing the 8:1 counter to count clock pulses following reset, which occurs as the 8:1 counter gate is reset. The 8:1 counter gate is divided into three stages consisting of flip-flops N603, N607 and N608 respectively.*

3-1.3.2. When SOW leaves the Buffer, the first data bit is shifted into the 1st bit of an 8 bit shift register (cores M502 through M509) in the Output Register Chassis. Following this action by 500 microseconds; the 8:1 counter counts to 1. Shift pulses (at 1 kc) continue to shift the data; each shift followed 500 microseconds later by the counter. When the 1st data bit is shifted into the 8th core of the Output Register, it is followed by a count of 8. This brings up the shift register gate level for one count, allowing the next shift pulse to read data out of the 8 cores in the Output Register into the storage flip-flops, N502 through N517. (The next 8 bit data word will not occur for another 8 milliseconds). If EOW, associated with the last 8 bits of data, occurs, it will leave the Buffer 5 milliseconds after the last data bit. The sample pulse will not be generated until approximately 6 milliseconds after the last data bit has occurred at the output of the Buffer. This allows the EOW flip-flops N308 in the Control Chassis to be set, if EOW occurs, before a sample pulse is generated. When EOW leaves the Buffer, it resets the 8:1 counter gate thereby inhibiting further sample or gating pulses. When additional data in the form of artificial "1's" appears on the data line following EOW, it is shifted through the Buffer, but is never gated into the Output Register flip-flops.

3-1.3.3. There are two flip-flops driven from each core in the Output Register to provide isolation and independent operation to the DCC's. In the event of failure in one section of the flip-flops, the remaining half will continue to furnish correct information to the DCC to which it is connected. The flip-flops are not reset until the 8th count of the 8:1 counter, which occurs 500 microseconds before new data is to be read in. This allows visual observation of the last word sent to the DCC, provided there is a sufficient time lapse between EOW and SOW outputs.

3-1.3.4. As already mentioned, data coming from a single source enters two individual Data Line Amplifiers via two separate lines with the data displaced in time. This data is re-aligned in the Buffer Chassis to the nearest half-millisecond, by delaying the leading data up to 16 milliseconds with respect to data on the trailing channel. As the data enters the Output Register, it is stored until one of the Timing Logic Chassis indicates that a sample pulse should occur by the 8th count of the 8:1 counter. The Control Chassis acts upon the first sample pulse request from either Timing Logic Chassis, and generates sample pulses to the sub-channel #1 or #2 of both DCC's after a delay of approximately 5.5 milliseconds. (Figure 9-2 illustrates the various connections of the Receiver to the DCC's.) A sample monitor circuit

*All discussions concerning Transistor Networks will be found in the Appendix of this manual.

in the Control Chassis monitors the output of the sample pulse circuitry, and will switch to redundant circuitry should sample pulses at the output cease to occur at regular intervals during the period between delayed SOW and delayed EOW. The occurrence of this condition illuminates the SAMPLE MONITOR indicator I302, on the front panel of the Control Chassis as a warning to operating personnel. The sample monitor is latching and must be reset by pressing the RESET pushbutton S310, to return it to its original monitoring state. Redundant circuitry is also provided for EOW, with a monitor circuit which switches to the redundant circuitry upon failure of the EOW pulse to occur at the output. The E.O.W. MONITOR indicator I301 is illuminated when redundant circuitry is in use.

3-1.3.5. Sample pulse and EOW must be generated from either receiver of a pair. This requires "OR" gating of the signals to produce a proper output. Without the monitoring circuitry with standby independent sample and EOW circuitry, a single failure in the "OR" gate could cause complete loss of data on both receivers of a pair.

3-1.4. Test Mode - The test switch, S302, labeled TEST PATTERN on the Control Chassis, has five positions: four producing automatic data patterns and the fifth for manual insertion of data. The four automatic patterns are: "1's, "0's," alternating "1's" and "0's," and alternating "0's" and "1's." In the manual position there are two pushbuttons, S304 and S301, labeled SHIFT, ONE and ZERO, which will insert a "0" or "1" in any desired sequence. Also under manual conditions, SOW and EOW pulses may be generated by pushbuttons S305 and S306, to put the system in and out of the operating mode. (Operating mode refers to the system's requirement for SOW before it will produce outputs to the DCC).

3-1.4.1. To start automatic generation of data in the test mode, it is necessary to switch the OPERATE TEST switch, S303, from the operate to the test position. This activates the 1 kc free running multivibrator (FRMV) which generates clock and data functions, and the one-shots which generate SOW and EOW. In the test mode, both Buffers of a pair of receivers should be set for the same delay via switch S401. To operate in the manual position, the system should be cleared by a manual EOW, followed by manual shifts until EOW is shifted out of the Buffer. This is dependent upon the setting of the Buffer Chassis. It is recommended that a "0" delay be used on the MILLISECONDS DELAY switch to reduce the number of pushbutton operations required. When EOW leaves the Buffer, the EOW indicators, DS301 and DS302, on the Control Chassis will light, and the SOW indicators, DS303 and DS304 will be extinguished. To insert a desired data pattern, it is then necessary to press the SOW button followed by a shift button. The operator may now insert any desired pattern of "1's" or "0's." (SOW indicators will illuminate and EOW indicators will be extinguished after the first bit of data is entered). Visual indication is provided as the bits appear on the Output Register indicators indicating the status of the lines to the DCC. It should be remembered, while inserting data, that the first 8 bits will not appear on the Output Register indicators until 9 bits have been

entered which is coincident with the first 8 bits entering in the Output Register flip-flops.

3-1.4.2. Each Output Register Chassis is designed to send identical data to two DCC's and the light patterns in the A and B row of each Output Register Chassis should be identical.

3-1.4.3. In the test mode (with the Buffers set for identical delays) the four rows of indicators on the Output Registers of a receiver pair should all have an identical pattern. A description of the test circuitry can be found under paragraph 3-3.1., Control Chassis.

3-2. DATA LINE AMPLIFIER, MEC MODEL 71-8A (See Appendix)

3-2.1. Data on all four channels entering the Model 72 Data Receiver initially enters the Data Line Amplifiers. The Data Line Amplifiers separate the incoming 2 kc tone bursts into SOW pulses, data pulses, and EOW pulses. The output data line will contain pulses for both SOW and EOW, and the SOW line will have a pulse for EOW. SOW entry is a 2.5 millisecond burst, Data a 0.5 millisecond burst, and EOW a 4.5 millisecond burst.

3-2.2. A detailed description of the MEC Model 71-8A Data Line Amplifier may be found in the Appendix of this manual.

3-3. CONTROL CHASSIS, MEC MODEL 72-3A (Figures 3-1, 9-6 and 9-7)

The Control Chassis contains the circuitry required for test operation, the sample pulse and EOW circuitry, and the monitoring circuitry for the sample pulses and EOW levels.

3-3.1. Test Circuitry - The clock for test mode (See Figure 9-6, Sheet 1) is derived from a 1 kc free running multivibrator (FRMV), N302. This circuit is inhibited during the operate mode by connecting pin 2 through a 10K resistor, R305, to +12 volts. The frequency of this multivibrator may be adjusted by potentiometer R307. The frequency will vary slightly with varying data patterns; however, this adjustment is not critical. An emitter follower N321 isolates the FRMV from the test circuitry. Its output, pin 3, is connected to clock and data inputs through test switches for a data pattern of all "1's". For a data pattern of all "0's" the output of N321 is connected to clock inputs only. For alternate "1's" and "0's" and "0's" and "1's", flip-flop N303 is used for data, and N321 is used for clock. (Switch positions for various test modes are shown in Figure 9-6, Sheet 1.) Operating on 1 kc from N321, the Control Chassis produces a 500 cycle waveform which inserts a "1" on the data line for every other clock pulse. The correct pattern is obtained by synchronizing SOW with one of the outputs (pin 8 of N303). The sequence is as follows: the rising edge at pin 7 of one-shot N306 triggers flip-flop N304 at pin 6, causing pin 8 to go to 0 volts. This allows the next positive going edge from pin 8 of N303 to trigger flip-flop N304 at pin 7. The output of N304, pin 5 now goes to 0 volts and generates a SOW pulse that is synchronized with the output at pin 8 of N303. After 200 milliseconds, pin 5 of N306, a 200 millisecond one-shot, goes positive and triggers one-shot N305. Pin 7 of N305 goes positive at this time and triggers flip-flop N322 at pin 6, causing pin 5 to go negative. On the next positive going pulse from pin 8 of N303, N322 is triggered at pin 7, the output at pin 5 goes positive, and sends the EOW pulse to the Buffer.

3-3.1.1. In the manual mode, SOW, EOW, and SHIFT ZERO are generated by pushbuttons S305, S306 and S301 respectively. SHIFT ONE is obtained from a 500 microsecond one-shot, N301, when triggered by pushbutton S304. The positive going leading edge of the output pulse from pin 7 of one-shot N301 triggers the data one-shot N613, in the Timing Logic Chassis. The output of N301 at pin 5 is used to generate a clock pulse to the Schmitt trigger in the Timing Logic Chassis, which produces a shift.

3-3.2. EOW Circuitry - (Figure 9-6, Sheet 2). Pins 15 and 16 of P301 are inputs from the EOW shift registers in the Buffer Chassis of one receiver pair. Each EOW input is connected to pin 3 of a 4 millisecond one-shot, N307 and N308 respectively. The positive going output at pin 7 of the one-shots is the output of an internal emitter follower. In this fashion, there is effectively a stage of isolation on each output line. The negative going output at pin 5 of N307 and N308 drives an amplifier, N309A and N309B respectively. The amplifier outputs are positive-going pulses similar to the pin 7 output of one-shots

N307 and N308. Only one of the two pairs (N307 and N309A or N308 and N309B) is connected to the output terminals, pins 32 and 33 of P301, at any one time. This is dependent upon the EOW monitor circuit and relay K301. This relay is normally energized and N307 and N309A are connected to the output terminals, pins 32 and 33 of P301. (See Figure 9-5 for EOW waveforms.)

3-3.2.1. When an EOW pulse occurs at the output of either Buffer of a receiver pair, in addition to driving the EOW one-shots, the first pulse to occur at pin 15 or 16 of P301 will trigger relay driver flip-flop N310 on pin 6 or 7 respectively, in a manner that will de-energize relay K301. If EOW circuits N307 and N309A are operational, a pulse will occur at pin 4 of amplifier N309A which will trigger one-shot N323 at pin 3. After one millisecond, pin 5 of one-shot N323 will go positive, triggering flip-flop N310 at pin 3, and restoring the energized condition of relay K301. The 100μfd capacitor C324 is used to hold in the relay during the time flip-flop N310 is off. If failure of N307 or N309A occurs, flip-flop N310 will not receive a pulse at pin 3, and relay K301 will drop out as capacitor C324 discharges. Should the Buffer Chassis be set so the EOW pulses occur further apart than the delay of one-shot N323 (approximately one millisecond), flip-flop N310 will be triggered off by the latter of the two EOW pulses and will not be restored until the system goes through a sequence of SOW and EOW which will again trigger one-shot N323. It is for this reason that the Buffer Chassis must be set for identical delays in test mode.

3-3.2.2. When relay K301 is de-energized, redundant EOW circuitry, N308 and N309B, is connected to the EOW output lines to the DCC through capacitor C322. This condition is visually indicated on the front panel of the Control Chassis with the monitor switch S308 in the AUTO position by the E. O. W. MONITOR indicator I301 being lit. Should EOW signals or the monitor circuitry for some reason become intermittent, and the relay drops in and out continually, it is possible to manually override the monitor circuit and lock in either A or B EOW output circuitry with the EOW monitor switch S308. Position A directly applies -20 volts to the relay coil and disconnects flip-flop N310. This connects the A EOW circuits, N307 and N309A, to the output lines. In this position, the indicator is activated through the switch contacts. When in position B, 0 volts is placed across the relay and the B EOW circuits N308 and N309B are connected to the DCC's. In this position, power is connected to the indicator through the relay contacts 9 and 14, indicating to the operator that the switch is not in AUTO and manual override is in use. The indicator has two purposes. In AUTO position it indicates the status of the relay (which circuitry is in use). In A or B, the indicator is intended to relate the fact that the monitor is in a manual position, and the switch position indicates which circuitry is in use.

SWITCH POSITION	MONITOR INDICATOR	SYSTEM INDICATION
A	Off-Abnormal	Failure of Lamp, Switch
A	On-Normal	A Circuitry connected to output
AUTO	Off-Normal	A Circuitry connected to output
AUTO	On-Normal	B Circuitry connected to output
B	Off-Abnormal	Failure of Lamp, Switch or Relay
B	On-Normal	B Circuitry connected to output

3-3.2.3. Testing of the EOW monitor is accomplished by setting EOW Monitor switch S308 in AUTO and opening the connection between N309A and N310 with pushbutton S307. When the pushbutton S307 is pressed, flip-flop N310 does not receive a pulse from one-shot N323 and is not re-set. The relay drops out and indicator I301 provides visual indication on the front control panel of the circuit status by lighting. Neon indicators DS301

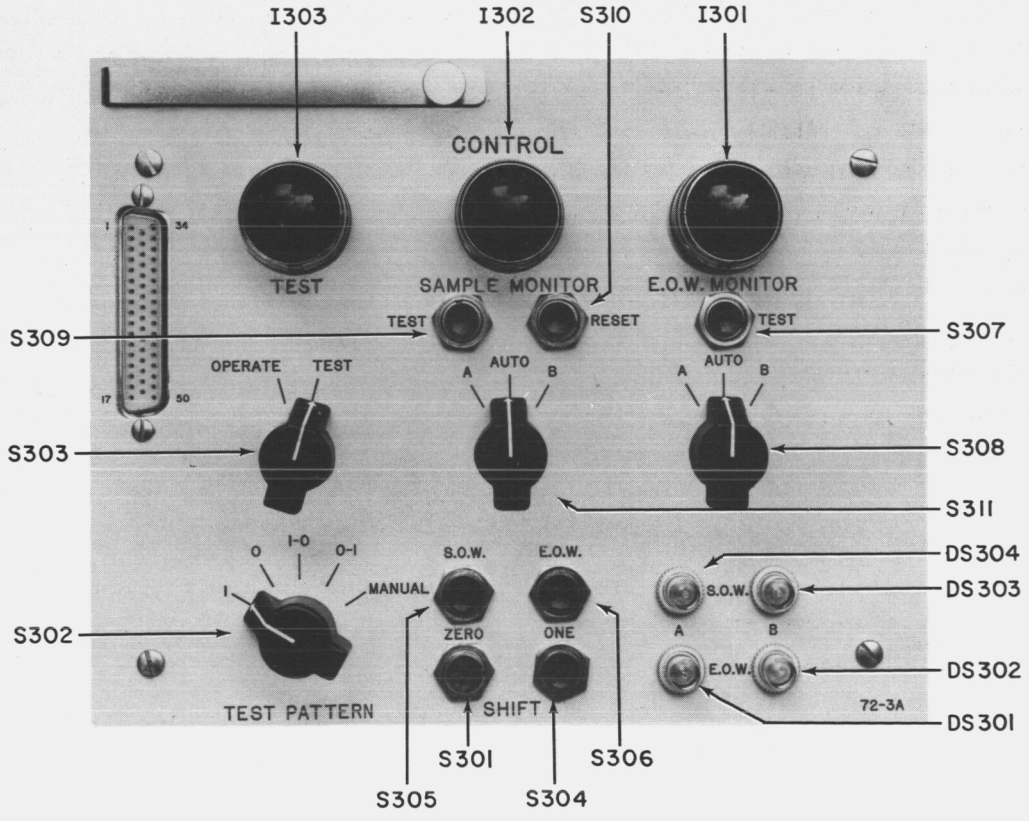


Figure 3-1. Control Chassis

and DS302 provide visual indication of EOW levels being sent to the DCC. If the A EOW circuitry is connected to the output, that is, when outputs from pin 7 of N307 and pin 4 of N309A signify EOW (at 0 volts), the neon indicators are lit. If the B circuitry is connected to the output lines, the EOW indicators indicate the status of N308 and N309B on outputs to the DCC. The connection of these indicators to the output lines are made through two 6.8K resistors, R335 and R336. The outputs to the DCC for the EOW levels are identical to those of the data levels in the Output Register. A description of these circuits is found under paragraph 3-5.2.

3-3.3. Sample Pulse Circuitry (Figure 9-6, Sheet 2) - Input pins 10 and 11 of P301 receive pulses from the sample pulse gates, one from each Timing Logic Chassis of a receiver pair. The input from pin 10 is connected to two isolating diodes CR309 and CR315. The input from pin 11 is similarly connected to diodes CR308 and CR316. The two inputs are then gated in two separate resistor-capacitor networks. Since they are identical, only one will be described. Resistors R337 and R339 provide a return path for capacitors C325 and C326 respectively, when diodes CR308 and CR309 are cut off. When one-shot N311 is in the steady state condition, its output at pin 5 is at 0 volts. Resistors R340 and R338 form a voltage divider which places the junction at about -2 volts; the voltage at pin 6 of N311 is approximately -.3 volts, thus keeping diode CR310 cut off. A positive pulse to either C325 or C326 causes CR310 to conduct, and triggers one-shot N311. Pin 5 of the one-shot then goes to -20 volts, biasing CR310 at -20 volts. As the input pulses to the gating circuit are slightly less than 20 volts, a pulse occurring before the one-shot time has completed will not affect its time constant. Upon receipt of the first sample request pulse from either A or B sample pulse gates, N311, a 5 millisecond one-shot, provides a delay, the duration of which allows the EOW pulse to occur. The EOW pulse will occur 5 milliseconds after the last data bit of a message. When N311 completes its time delay, its output triggers N312, a 10 microsecond one-shot. N312 in turn drives two emitter followers N313A and N313B, whose outputs, pins 3 and 6 respectively, are connected to normally open contacts 8 and 10 of relay K302.

NOTE

In referring to relay contacts the term "normally open" implies the condition of the contacts when the relay is de-energized. This is a descriptive usage only, as the relay under discussion may be energized under normal operating circumstances.

When this relay is energized, causing the contacts to close, these outputs are connected to pins 26 and 28 of P301 which are sample pulse lines to the DCC. (See Figure 9-5 for sample pulse waveform.) Redundant circuitry for generating sample pulses is connected to normally

closed contacts 1 and 9 of relay K302. This circuitry parallels the operation just described. It consists of N318, N319 and N320A and B.

3-3.3.1. The sample pulse monitor circuitry is composed of N314, N315A, N315B, N316 and N317. N315A is an amplifier controlled by the 8:1 counter gate in the Timing Logic Chassis. Its output at pin 4 is approximately +10 volts when its input at pin 2 is negative during the period between EOW and SOW. This output holds the input of one-shot N316, pin 6, positive, via timing capacitors C330 and C342, thereby keeping the output, pin 5 at -20 volts. At the departure of SOW from the Buffer, the input of N315A goes to 0 volts and the output goes to -20 volts, therefore, N316 is dependent upon pulse amplifier N315B to keep its input, pin 6, positive by holding the timing capacitor positive. Each time a sample pulse appears at the output of N313B, it triggers N314, a 5 millisecond one-shot, at pin 3. This one-shot drives pulse amplifier N315B at pin 7, continually charging the timing capacitors of N316 each time a sample pulse occurs. As long as the sample pulses continue, the timing capacitors are recharged, prohibiting a positive pulse at the output (pin 5) of N316. Should sample pulses fail to occur, one-shot N316 will complete its time delay, triggering flip-flop N317, which in turn removes power from relay K302. As a result, the sample pulse outputs to the DCC are switched from N313A and B to N320A and B. At the same time the relay drops out, the red SAMPLE MONITOR indicator on the Control Chassis lights, indicating the status of the relay. Facilities for testing the sample monitor are provided on the front panel of the Control Chassis. The pushbutton TEST switch S309 interrupts sample pulses to the sample monitor. When pulses fail to reach N314, flip-flop N317 is triggered, and the relay drops out. N317 must then be manually reset with pushbutton S310.

3-3.3.2. For both the sample monitor and the EOW monitor, there are provisions on the Control Chassis for overriding the automatic operation of the monitor circuit. In the A position, the relays of the monitor circuits are energized; in the B position, they are de-energized. In either of the manual positions the indicator lights are lit. Should Power Supply A fail, the relays of the monitor circuits in the Control Chassis A would lose power. When they drop out, however, they are connected to the circuits operating off the B supply. The same situation exists in Control Chassis B if Power Supply B fails. Failure of either supply with monitors in AUTO will not cause permanent loss of sample or EOW outputs to the DCC.

3-3.3.3. There are two neon indicators, provided on the front panel of the Control Chassis, indicating the status of the 8:1 counter gate flip-flops in the Timing Logic Chassis which receives the SOW pulses and EOW pulses from the Buffer. These indicators are normally lit between SOW and EOW pulses from the Buffer Chassis. Data entering the system, such as artificial "1's", used for maintaining proper oscillator frequency during periods of data absence, will not generate sample or gating pulses within the system when the lights indicate the flip-flop is now in the EOW state. The EOW indicators represent the status of the

two EOW lines to the A and B DCC's. The status of the EOW monitor relay determines which circuits are connected to the lines. The EOW indicators are normally lit when the SOW indicators are off.

3-3.3.4. In the manual operation, the SOW indicators will light as a SOW pulse leaves the Buffer (which is the second shift after pressing the SOW button) and will stay lit until EOW pulses leave the Buffer, (the first shift after pressing the EOW button), at which time the EOW indicators will light.

3-4. BUFFER CHASSIS, MEC MODEL 72-4A (Figures 3-2, 9-8 and 9-9)

3-4.1. The Buffer Chassis provides delays for data, SOW and EOW, collectively in increments of one millisecond, for the purpose of aligning data received from a source which has initially delayed one channel of a pair with respect to the other. The delay also makes it possible to allow for additional delays that may occur due to routing of the data within the Receiver. Maximum possible delay is 16 milliseconds. Delay is accomplished by switching inputs from the Data Line Amplifier or test circuitry to pin 3 of the desired cores in the shift registers. One-shots for insertion of data and SOW are located in the Timing Logic Chassis. They are N613 for data and N611 for SOW. EOW, however, is inserted by one-shot N404 in the Buffer Chassis. The input at pin 6 receives actual or test EOW from the Control Chassis. The 10K resistor, R401, at the input, is utilized for termination of the EOW cathode follower in the Data Line Amplifier when in the operate mode.

3-4.2. Since shift pulses occur at a 1 kc rate, information is delayed in one millisecond increments between the time it enters and leaves the Shift Register by effectively increasing the number of cores in the string. This is accomplished by switch S401. A separate string of cores is used for data (M401 through M417); SOW (M418 through M435); and EOW (M436 through M452). (See Fig. 9-5 for typical "1" output of cores.) Each string is driven by a TN130B core driver, labelled N401, N402 and N403 respectively.

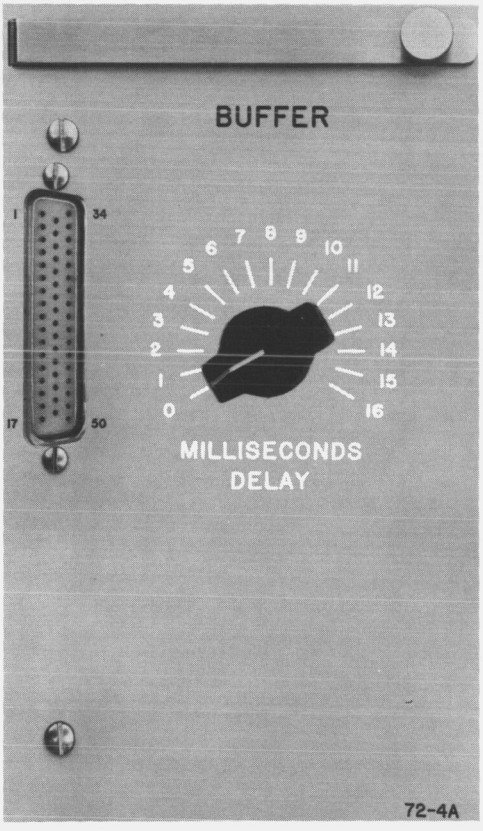


Figure 3-2. Buffer Chassis

The core drivers shift when activated by a pulse received at pin 2 of P401, which is clock, phase 2, from the Timing Logic Chassis. The shift pulses are generated between gating functions derived from the 8:1 counter. As the 8:1 counter operates on clock, phase 1, it changes state 500 microseconds before or after shift pulses.

3-4.3. The SOW shift register has one more core at the output than the data and EOW registers. This core, M435, provides one additional millisecond of delay for SOW from the Buffer. This additional delay is necessary for properly starting the 8:1 counter in the Timing Logic Chassis, thereby insuring that the shift register gating pulse to the Output Register occurs at the proper time.

3-4.4. The output of the EOW shift register, pin 9 of core M452, is connected to one leg (CR404) of an "OR" gate consisting of diodes CR404 and CR405 (located in the Buffer Chassis) and resistor R632 (located in the Timing Logic Chassis). The EOW shift register output is also connected to pin 24 of plug P401. Pin 24 is connected through rack wiring to pin 42 of P401 of the Buffer Chassis belonging to the mating receiver. Thus, the second input to the "OR" gate is supplied from the EOW shift register of the mating receiver to diode CR405. Therefore, both Buffer Chassis contain "OR" gates which produce an output as a result of EOW from either EOW shift register of the mating receiver. The purpose of this circuit is to supply an EOW input to the Control Chassis and the Timing Logic Chassis should some malfunction occur to either receiver of the pair.

3-5. OUTPUT REGISTER CHASSIS, MEC MODEL 72-5A (Figures 3-3, 9-10 and 9-11)

3-5.1. Data from the output of the data shift register in the Buffer enters an 8 bit shift register, M502 through M509, in the Output Register Chassis. Shift pulses to core driver N501 are derived from the same phase 2 of clock that shifts the Buffer. 500 microseconds after a complete group of 8 bits enters the 8 bit shift register, such that the 1st bit is stored in M309, the gating level from the Timing Logic Chassis entering pin 2 of P501, rises from -20 volts to 0 volts for one millisecond. During this period, the next shift pulse to occur reads the data out of the shift register into storage flip-flops N502 through N517, each core driving 2 flip-flops. The gating level is connected to pin 5 of each of the eight cores. This is one side of the auxiliary winding. When a core is shifting out a "1" the other side of the auxiliary winding, pin 4, goes positive approximately 8 volts. When the gating level is at -20 volts, a "1" appearing at pin 4 does not go above ground and does not set the flip-flops. (See Figure 9-5 for shift register gate wave forms). When the gating level goes to approximately -2 volts, a positive 8 volt pulse at pin 4 of a core goes well above ground and will set the two flip-flops to which it is connected. A "0" having been shifted from a core, is approximately a +0.5 volt pulse and does not rise above ground when referenced to -2 volts. Resistors R537 and R501 provide -2 volt bias when the input goes to 0 volts at pin 2 of P501. At the same time the gating pulse goes positive, the storage flip-flops are reset by a pulse from the Timing Logic Chassis which enters the Output Register on pin 4 of P501.

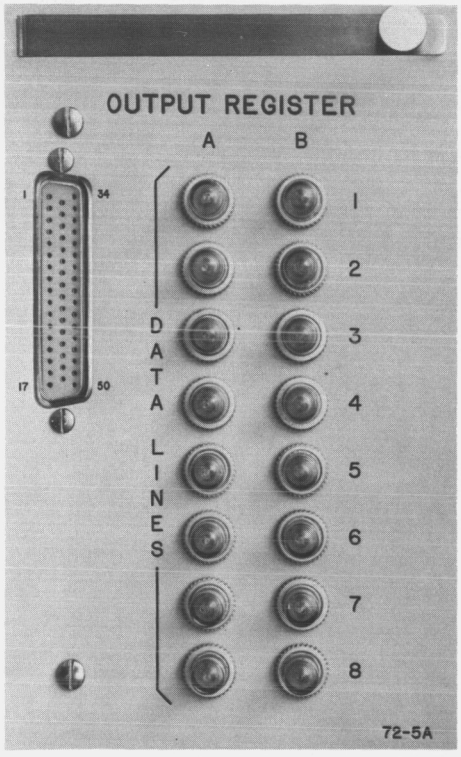


Figure 3-3. Output Register Chassis

3-5.2. The Output Register flip-flops are TN144's with a diode clamp to ground on the output which prevents the output from going positive. To avoid the output swinging below ground under loading, a resistor such as R503 is returned to a positive voltage from each flip-flop thus maintaining the diode in a clamped state. (See Figure 9-5 for waveform of a typical Output Register flip-flop). A neon indicator is provided on the output of each flip-flop. The indicator is lit for 0 volts, indicating a "1", and is off for -10 volts, indicating a "0". In the lower left hand corner of Figure 9-10 is a table calling out the DCC location of each Output Register Chassis output.

3-6. TIMING LOGIC CHASSIS, MEC MODEL 72-6A (FIGURES 3-4, 9-12 and 9-13)

3-6.1. In addition to aligning 2 channels of data from a single source that have been deliberately misaligned, the Data Receiver must send its outputs to the DCC in groups of 8 bits. It must ignore anything on the input line between EOW of one data message and SOW of the following data message. The Timing Logic Chassis provides these functions. Clock (1 kc) enters the Timing Logic Chassis on pin 1 of P601 from the Control Chassis. If it is actual data it is in the form of a sine wave. In test mode it is a differentiated square wave. Schmitt trigger N601 shapes the clock pulse. Its output at pin 5 is out of phase with the input at pin 3. Potentiometer R609 and emitter follower N605 are used to bias N601, causing the Schmitt trigger to trigger as the input crosses 0 volts. The output of the Schmitt trigger drives a variable one-shot N614 at pin 3. This one-shot is adjusted by varying potentiometer R603 to place shift pulses approximately between the data bits entering the Receiver. This delay is nominally 160 microseconds. N614 triggers a 500 microsecond one-shot, N602, which generates the 2 phases of the clock pulse that are used within the system. Clock, phase 1, from pin 5 of N602 triggers the first stage (N603) of the 8:1 counter. Pin 7 of N602 (clock, phase 2) is connected to pins 2 and 3 of P601 which go to the core drivers in the Buffer and Output Register Chassis. The 8:1 counter consists of flip-flops N603, N607, and N608.

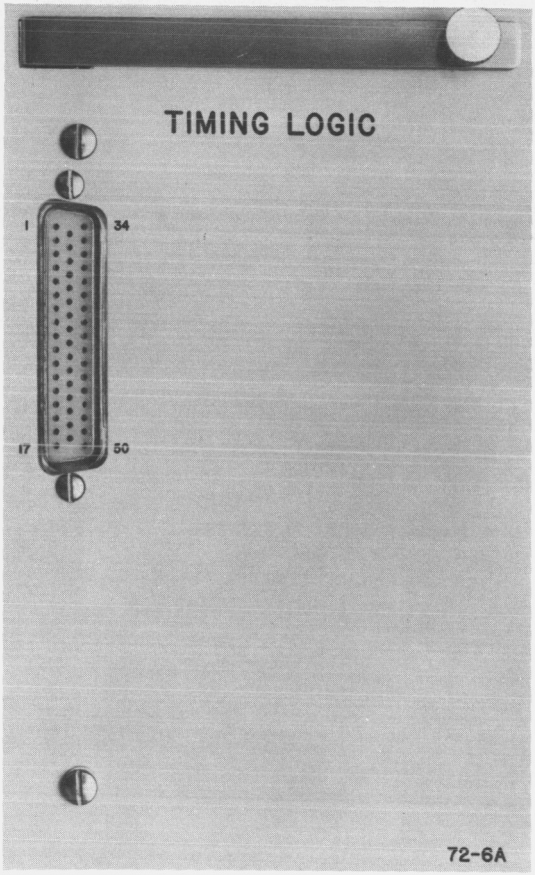


Figure 3-4. Timing Logic Chassis

3-6.2. The output, pin 5, of the first stage of the counter, N603, is a 500 cycle square wave. N607 is the second stage which counts down the 500 cycle square wave and produces a 250 cycle square wave at pin 5 which drives the third stage, N608. The output of N608 is a 125 cycle square wave. The three stages of the 8:1 counter are reset at pin 7 by a positive pulse from flip-flop N606 which occurs each time a SOW pulse is received from the Buffer. Clock pulses are inhibited from triggering N603 by the 8:1 counter gate, flip-flop N606, when it receives a delayed EOW pulse from the Buffer. The inhibit is removed when N606 is triggered by a delayed SOW pulse from the Buffer. (Figure 9-5 shows the waveform of the 8:1 counter gate.) Upon receiving a SOW pulse, the 8:1 counter operates on clock 1. The output of N608, pin 5, goes positive when the count of 8 is reached. This triggers flip-flop N610, bringing the shift register gate level to 0 volts and allowing data to be read into the Output Register flip-flops. N610 in turn drives N604 and N609A. N604 is the flip-flop used to generate sample pulses in the Control Chassis. N609A is an emitter follower which resets the Output Register flip-flops on the count of 8, 500 microseconds prior to the shifting of new data from the cores. Flip-flops N604 and N610 are both reset by the following count of 1 from N603. Their outputs are a positive level of 0 volts for one millisecond between the counts of 8 and 1 of the 8:1 counter, during the period between delayed SOW and EOW from the Buffer. Figure 9-5 shows the waveform of flip-flop N610, referred to as the shift register (S.R.) gate.

3-6.3. The gating resistors R620 and R628 at pin 3 of N610 insure that N610 is not triggered by N608 when the counter is reset at delayed SOW.

3-6.4. One-shots N611 and N613 insert SOW and data into their respective shift registers in the Buffer Chassis. They operate on a pulse either from the test circuitry or the Data Line Amplifier, depending upon the position of the OPERATE TEST switch on the Control Chassis. The resistors, at their input, provide cathode resistors for the cathode followers in the Data Line Amplifiers.

3-6.5. Should some malfunction occur and the Timing Logic Chassis not receive an EOW pulse from its own Buffer Chassis, the Buffer Chassis of the paired receiver will supply an EOW pulse through the "OR" gate composed of diodes CR404 and CR405 in the Buffer Chassis and resistor R632 located in the Timing Logic Chassis.

3-7. POWER CONTROL CHASSIS, MEC MODEL 72-7A (FIGURES 3-5, 9-14 and 9-15)

3-7.1. The Power Control Chassis provides the means for switching a-c power to the rack, measurement of all internally generated voltages, and contains indicators to provide a visual detection of power failures.

3-7.2. AC power is switched to the rack via switch S701. When power is on, neon indicator DS701 is on. Diode CR701 rectifies the a-c for measurement. Meter MV701 and switch S702 are used to measure 120 vac, the 3 d-c voltages from both the A and B supplies (+12 volts, -20 volts, and -85 volts) and the +250 volts and -250 volts generated within each of the four Data Line Amplifiers. MV701 is a 1.2 ma meter. By limiting the current from each voltage to 1 ma with an appropriate 1% resistor, all voltages read approximately "10" on the meter, representing 100% when they are properly adjusted. For optimum usage of the meter, however, the procedure in the following paragraph is recommended.

3-7.3. Using an external meter such as a Simpson Model 270 or Triplett Model 630, correctly set each of the 3 d-c voltages of both supplies. The voltages are brought out at the front of the supply and clearly identified via test jacks TJ401 through TJ404. Record the reading of panel meter MV701 for all voltages on the VOLTAGE SELECTOR switch. The recorded readings may now be used to determine any discrepancy of the system voltages.

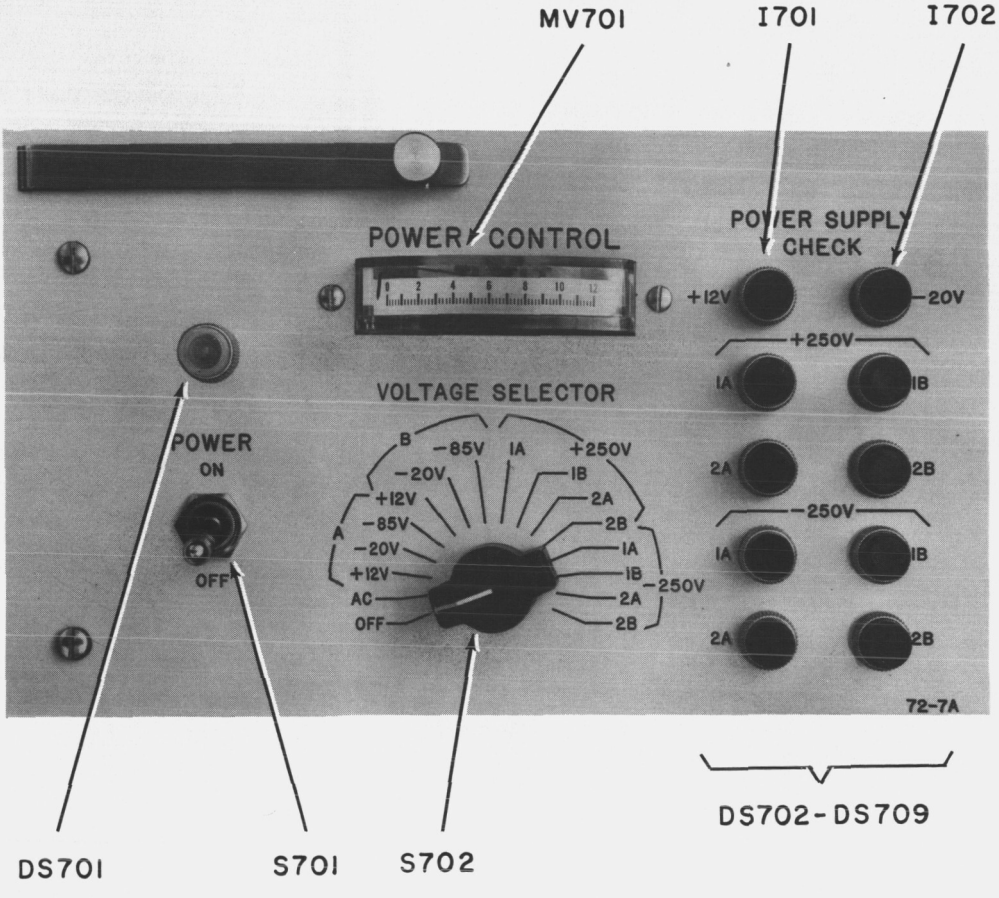


Figure 3-5. Power Control Chassis

3-7.4. In addition, indicators I701 and I702 are between the two -20 volt and +12 volt lines respectively, providing a visual indication of failure of either one of the two lines. Failure of both lines however, will not give an indication. Series resistor R723 is used on the -20 volt indicator to allow use of the same type lamp in both indicators.

3-7.5. There are eight neon indicators provided for monitoring the +250 volts and -250 volts from the Data Line Amplifiers. One group will be described. The four +250 volt lines are "OR" gated through CR702, CR703, CR704 and CR705. The common point of these diodes provides power to all four of the indicators, DS702, DS703, DS704 and DS705 through 100K limiting resistors. As long as there is no power failure, each indicator has +250 volts applied to both sides and remains extinguished. Should one supply fail, one side of the neon loses +250 volts and lights. A ground path is provided, in case the Power Supply failure is an open, with 100K resistors to ground.

CHAPTER IV

OPERATION

4-1. When all rack connectors are properly connected and a-c power is supplied to the Receiver, place a-c power switch S1, located at the rear of the rack, to the ON position. A red indicator I1, adjacent to the switch, indicates when power is on (see Figure 4-1). This switch controls a-c power to the Power Control Chassis, MEC Model 72-7A. Switch on a-c power to the system via S701, located on the front panel of the Power Control Chassis. A neon indicator DS701, located above the switch, indicates when power is on. Power indicators on each of the Data Line Amplifiers will be lit at this time.

4-1.1. In checking voltages to the system, the voltage to be checked is selected with switch S702 on the Power Control Chassis. AC should indicate "10" ±10%. After following the procedure in paragraph 3-7.3, the +12 volts, -20 volts, and -85 volts should indicate the recorded readings ±3%. The +250 volts should indicate "9.5" ±3%; the -250 volts should indicate "10" ±3%.

NOTE

The designation A refers to the right hand supply; B, the left hand supply. The designation for the 250 volts from the Data Line Amplifiers are 1A, 1B, 2A, 2B, from left to right.

Should failure occur to either of the +12 volt or -20 volt supplies, red indicators I702 and I701 on the Power Control panel will light, respectively. Failure of the -85 volt is obvious as all neon indicators are operated from this voltage. There is an indicator provided for each of the +250 volts and -250 volts generated within the Data Line Amplifiers.

4-2. Switch the TEST OPERATE switch on the Control Chassis to TEST. If already in test, switch to OPERATE and back to TEST. Set the Buffers for identical delays. Set the monitors in AUTO. Select a test pattern. The pattern should appear on the Output Register indicators. The SOW and EOW indicators should be alternating, with the SOW period about four times as long as the EOW period. The A and B indicators should be operating in unison. Test monitor circuits by pressing the monitor test pushbuttons. The indicators will light when the test pushbuttons are pressed. (It is necessary to reset the sample monitor after testing.)

4-2.1. Check all four test patterns. The sample monitor may operate when changing patterns, but should remain off after it is reset. The preceding operations should be done for both receiver pairs. Indications of difficulty or improper Data Line Amplifier adjustments are:

1. A and B EOW indicators operate in unison, but SOW indicators do not.
2. EOW monitor frequently lights momentarily. (If data is satisfactory on both lines and no spurious noise pulses exist, or temporary drops in level, etc., the indicator would not light at all.)
3. Sample Monitor or EOW monitor indicator operates and does not reset.
4. EOW neon indicators stay on when monitor is in A or B position.
5. EOW and SOW indicators do not maintain normal sequence.
6. Adjacent Output Registers of a receiver pair do not have identical data patterns.

4-3. It is assumed that the Data Line Amplifiers are properly adjusted. If this is not the case, they should be adjusted as described in paragraph 2-8 in DATA LINE AMPLIFIER, APPENDIX. To properly align the data, it is necessary to adjust the Buffer delays. This is accomplished by using a dual-trace oscilloscope and observing both EOW pulses as they leave the Buffer. (Pin 8 at the test jack of both Buffers of a receiver pair.) Synchronize the scope on one of the two pulses. If the leading EOW is selected, both pulses will appear on the scope displaced by not more than 16 milliseconds. If not, the sync should be switched to the remaining EOW pulse. The delay switch of the Buffer with the leading pulse should then be adjusted until the two pulses are within one millisecond of each other. When this is done, it should be determined if the pulses are more than 500 microseconds apart. If they are, an additional millisecond of delay should be added to the Buffer that is being set. Following this, switch the sync to the other EOW pulse (the leading pulse is now on the other line) and verify that the EOW pulses are now less than 500 microseconds apart.

4-4. When operating properly with data from the B-GE computer, the SOW and EOW indicators will repeat a sequence of SOW, a short EOW; SOW, a long EOW. The data from the IP709 repeats a sequence similar to that of the test mode. In both receiver pairs, the only data output to the Computer that is easily determined visually on the indicators of the Output Registers is the last 8 bits, as this data remains on the lines until new data comes in.

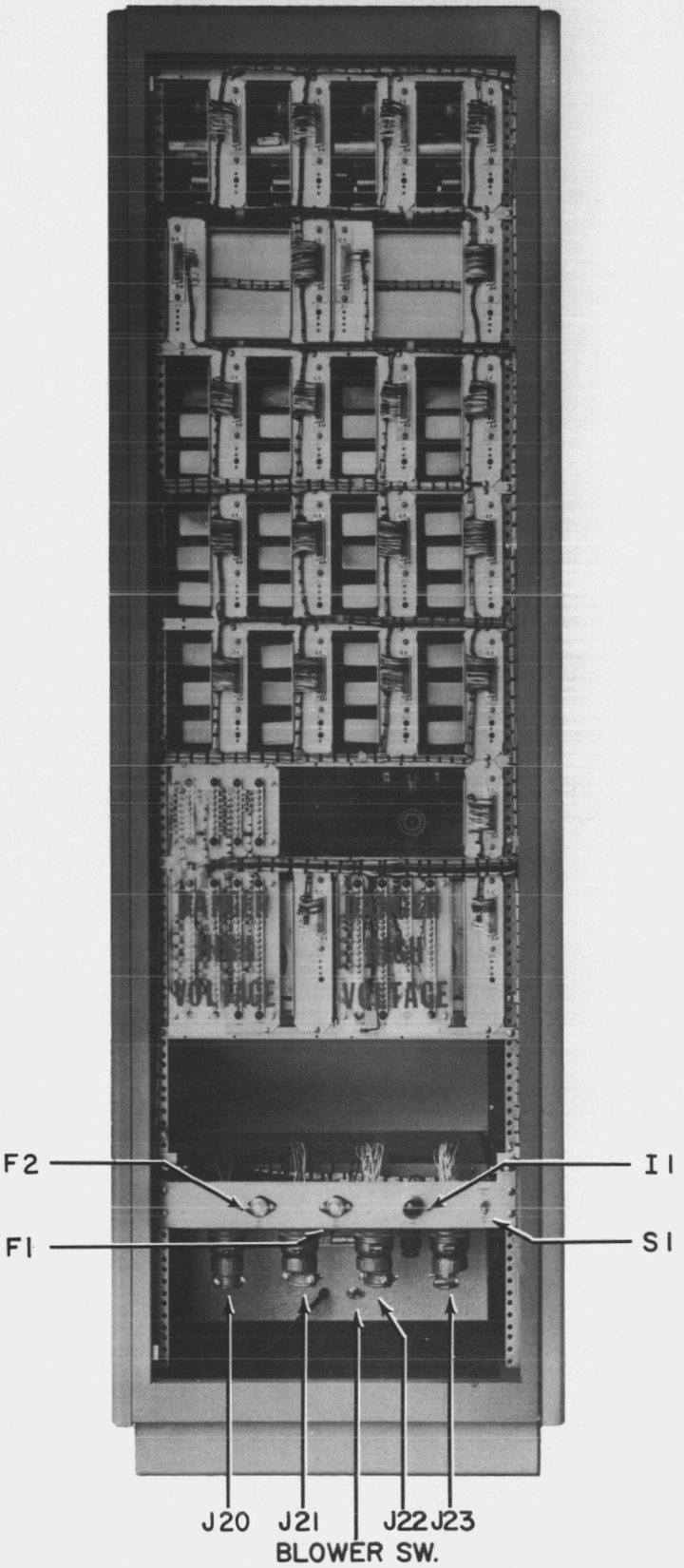


Figure 4-1. MEC Model 72 Data Receiver, Rear View

CHAPTER V
INSTALLATION

5-1. Provisions should be made to supply the Model 72 Data Receiver with 120 vac 60 cycles, single phase at approximately 8 amperes as power inputs. The Receiver receives a-c power through J33 at the rear of the rack. Internal connection information is as follows:

INPUT - OUTPUT CONNECTORS

CONNECTOR	TYPE	DESCRIPTION	MATING CONNECTOR
J20-J23	MS3102A-32-7P	Data Line Outputs	MS3106B-32-7S
J33	MS3102A-18-11P	Power Input	MS3106B-18-11S
*J34-J41	N60-R3-A	Data Line Inputs	N60-P2-2
J42	MS3106B-20-15S	Recorder Inputs	MS3102A-20-15P

5-2. The rack should be installed on a reasonably flat surface and if it is to be installed near a wall, its rear portion should not be less than three feet from the wall. This enables easy access to the rack through the rear door.

5-3. Adjustments and procedures to be executed prior to operating the equipment will be found in CHAPTER IV, OPERATION. Wire size and cable information will be found in CHAPTER VIII, WIRE LIST.

*Connectors J34-J41 are utilized as pairs for each of the four data lines.

CHAPTER VI

MAINTENANCE

6-1. No special considerations are needed for maintenance of this equipment. However, normal failures of individual components may be expected and can be located through normal maintenance operations. Values of all major component parts used in the chassis are indicated in CHAPTER VII, PARTS LIST. The indicators located on the front panels of the chassis give indication of malfunction in most cases. By observing these indicators during normal operation, it is possible to determine quickly in which chassis the trouble is located, and in which portion of the chassis the trouble is contained.

6-2. The only preventive maintenance necessary is the cleaning of the Blower filter approximately once every thirty days. The filter should be removed and cleaned in a solution of warm water and detergent. Periodic tube testing, either with a tube tester, or by merely substituting known good tubes, should be carried out. If relays, or other electro-mechanical devices do not function properly with normal adjustments, the complete sub-assembly should be replaced, and the malfunctioning unit returned to the manufacturer for possible repairs.

6-3. It is strongly urged that this manual be thoroughly read and completely understood before operating the equipment.

CHAPTER VII

PARTS LIST

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
1-1				MEC 72-1AAA	ASSEMBLY, CONNECTOR BRACKET	1		
1-2	F1, F2			Bussmann BAN	FUSE, 10 Amp	2		
1-3	I1			Dialight 6S6	LAMP, Incandescent, Candelabra Base, 125V, Clear	1		
1-4	J20-J23			Cannon MS3102A-32-7P	CONNECTOR	4		
1-5	J33			Cannon MS3102A-18-11P	CONNECTOR	1		
1-6	J34-J41			Nugent N60-R3-A	CONNECTOR	8		
1-7	S1			Cutler Hammer ST52N	SWITCH, Toggle, DPDT	1		
1-8	TB1			Cinch Jones 2-140	TERMINAL STRIP	1		
1-9	XF1-XF2			Bussmann HPC	FUSE HOLDER	2		
1-10	XI1			Dialight 514001-111	INDICATOR HOLDER	1		
3-1				MEC 72-3A	ASSEMBLY, CONTROL			
3-2	C321-C323			Cornell Dubilier PM4S1	CAPACITOR, FIXED MYLAR, .01µf, 400vdc	3		
3-3	C301-C303 C311 C314 C328 C335			MIL CM-19B-102K	CAPACITOR, FIXED MICA, 1000µµf, 10%, 500 vdc	7		
3-4	C304			Cornell Dubilier PM4S5	CAPACITOR, FIXED MYLAR, .05µf, 400vdc	1		
3-5	C305 C306 C341			Cornell Dubilier PM4S2	CAPACITOR, FIXED MYLAR, .02µf, 400vdc	3		
3-6	C307 C324			Fansteel F308-1	CAPACITOR, (Blu-Cap), 100µf, 30vdc	2		
3-7	C308			Fansteel F215-1	CAPACITOR, (Blu-Cap), 10µf, 100vdc	1		
3-8	C316			MIL CM-19B-331K	CAPACITOR, FIXED MICA, 330µµf, 10%, 500 vdc	1		
3-9	C310			MIL CM-19B-681K	CAPACITOR, FIXED MICA, 680µµf, 10%, 500 vdc	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
3-10	C312 C309 C325 C326 C332 C333			MIL CM-19B-471K	CAPACITOR, FIXED MICA, 470μμf, 10%, 500 vdc	6		
3-11	C313			G.E. 29F571-G4	CAPACITOR, Tantalytic, 6μf, 50vdc	1		
3-12	C315			G.E. 29F567-G4	CAPACITOR, Tantalytic, 20μf	1		
3-13	C331			MIL CM-19B-152K	CAPACITOR, FIXED MICA, 1500μμf, 10%, 500 vdc	1		
3-14	C327 C329 C334			Cornell Dubilier PM4P5	CAPACITOR, FIXED MYLAR, .5μf, 400vdc	3		
3-15	C330			G.E. 29F562-G4	CAPACITOR, Tantalytic, 3μf, 25vdc	1		
3-16	C338 C339			MIL CM-19B-561K	CAPACITOR, FIXED MICA, 560μμf, 10%, 500 vdc	2		
3-17	C340			Cornell Dubilier PM4P1	CAPACITOR, FIXED MYLAR, .1μf, 400vdc	1		
3-18	C342			G.E. 29F580-G4	CAPACITOR, Tantalytic, 1μf, 75vdc	1		
3-19	C343 C344			Cornell Dubilier PM2P47	CAPACITOR, FIXED MYLAR, .47μf, 200vdc	2		
3-20	CR301 CR306- CR319 CR321 CR322 CR326 CR327			Clevite CTP-503 or T12G	DIODE	19		
3-21	CR320			Hoffman 1N703	DIODE	1		
3-22	DS301- DS304			MEC 16-101	INDICATOR, Neon	4		
3-23	I301- I303			Dialight Corp. 6S6-125V	LAMP, INCANDESCENT, Candelabra Screw Base Clear	3		
3-24	K301 K302			C.P. Clare RP4461-G28	RELAY (4P or m C), Type 2	2		
3-25	N323			MEC TN138	TRANSISTOR NETWORK	1		
3-26	N301 N316 N312 N319			MEC TN111	TRANSISTOR NETWORK	4		
3-27	N302			MEC TN57	TRANSISTOR NETWORK	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
3-28	N303 N304 N322			MEC TN90B	TRANSISTOR NETWORK	3		
3-29	N305- N308 N311 N314 N310			MEC TN138B	TRANSISTOR NETWORK	7		
3-30	N310 N317			MEC TN79	TRANSISTOR NETWORK	2		
3-31	N313 N315 N320 N309 N321			MEC TN50	TRANSISTOR NETWORK	5		
3-32	P301 P302			Cannon DD-50P	PLUG, Male, 50 Pin Contact, 5 Amp Rating	2		
3-33	R301 R304 R313- R315 R338 R350			MIL RC20GF104K	RESISTOR, FIXED COMPOSITION, 100K, 10% 1/2W	7		
3-34	R302			MIL RC20GF563K	RESISTOR, FIXED COMPOSITION, 56K, 10%, 1/2W	1		
3-35	R303 R308 R332 R337 R339 R349 R351 R333			MIL RC20GF223K	RESISTOR, FIXED COMPOSITION, 22K, 10% 1/2W	8		
3-36	R305 R311 R312 R325 R329 R327 R364 R326 R330 R340 R345 R352			MIL RC20GF103K	RESISTOR, FIXED COMPOSITION, 10K, 10% 1/2W	12		
3-37	R306 R357			MIL RC20GF473K	RESISTOR, FIXED COMPOSITION, 47K, 10% 1/2W	2		
3-38	R307			Allen Bradley JA1L040S253UC	POTENTIOMETER, 25K, 2W, Linear Taper	1		
3-39	R309 R310 R343 R347			MIL RC20GF332K	RESISTOR, FIXED COMPOSITION, 3.3K, 10% 1/2W	4		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
3-40	R321 R324 R328 R331 R346 R358			MIL RC20GF562K	RESISTOR, FIXED COMPOSITION, 5.6K, 10% 1/2W	6		
3-41	R334 R341 R342 R353 R354			MIL RC20GF102K	RESISTOR, FIXED COMPOSITION, 1K, 10% 1/2W	5		
3-42	R335 R336			MIL RC20GF682K	RESISTOR, FIXED COMPOSITION, 6.8K, 10% 1/2W	2		
3-43	R344 R348			MIL RC42GF561K	RESISTOR, FIXED COMPOSITION, 560 ohms, 10% 2W	2		
3-44	R355 R356			MIL RC20GF273K	RESISTOR, FIXED COMPOSITION, 27K, 10%, 1/2W	2		
3-45	R365 R366			MIL RC20GF822K	RESISTOR, FIXED COMPOSITION, 8200 ohms, 10%, 1/2W	2		
3-46	R362 R363			MIL RC20GF151K	RESISTOR, FIXED COMPOSITION, 150 Ohms 10%, 1/2W	2		
3-47	S301 S304- S307 S309 S310			Micro 2PB11	SWITCH, PUSHBUTTON	7		
3-48	S308 S311			Centralab PA2007	SWITCH, ROTARY, Non shorting	2		
3-49	S303			Centralab PA2035	SWITCH, ROTARY, Non shorting	1		
3-50	S302			Centralab PA2021	SWITCH, ROTARY, Non shorting	1		
3-51	TJ301			Cannon DD-50S	CONNECTOR, Female, 50 pin contact, 5 amp rating	1		
3-52	XI301- XI303			Dialight Corp. 514001-111	INDICATOR HOLDER	3		
3-53	XK301- XK302			Eby 9759-5	SOCKET, 14 Pin Miniature	2		
3-54	XN301- XN323			JAN TS101P01	SOCKET, Tube, Octal	23		
3-55				Whitso K-105	KNOB	4		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
4-1				MEC 72-4A	ASSEMBLY, BUFFER			
4-2	C401			Fansteel F110-1	CAPACITOR, (Blu-Cap), 10μf, 25vdc	1		
4-3	C402-C404			Fansteel F308-1	CAPACITOR, (Blu-Cap), 100μf, 30vdc	3		
4-4	C405			MIL CM-19B-272K	CAPACITOR, FIXED MICA, 2700μμf, 500vdc, 10%	1		
4-5	CR401-CR405			Clevite CTP-503 or T12G	DIODE	5		
4-6	M453-M455			MEC MN-13	MAGNETIC CORE	3		
4-7	M401-M452			MEC MN-11	MAGNETIC CORE	52		
4-8	N401-N403			MEC TN130B	TRANSISTOR NETWORK	3		
4-9	N404			MEC TN138B	TRANSISTOR NETWORK	1		
4-10	P401			Cannon DD-50P	PLUG, Male, 50 pin contact, 5 amp rating	1		
4-11	R402			MIL RC20GF182K	RESISTOR, FIXED COMPOSITION, 1800 ohms, 10%, 1/2W	1		
4-12	R401 R403 R404			MIL RC20GF103K	RESISTOR, FIXED COMPOSITION, 10K, 10% 1/2W	3		
4-13	S401			Oak 399655-MF	SWITCH, ROTARY, 3 Pole, 24 Position	1		
4-14	TJ401			Cannon DD-50S	CONNECTOR, Female, 50 pin contact, 5 amp rating	1		
4-15	XM401-XM455			JAN TS103P02	SOCKET, Tube, 9 Pin Miniature	55		
4-16	XN401-XN404			JAN TS101P01	SOCKET, Tube, Octal	4		
4-17				Whitso K-105	KNOB	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
5-1				MEC 72-5A	ASSEMBLY, OUTPUT REGISTER			
5-2	C501			Fansteel F110-1	CAPACITOR, (Blu Cap), 10μf, 25vdc	1		
5-3	C502 C503			Fansteel F308-1	CAPACITOR, (Blu Cap), 100μf, 30vdc	2		
5-4	C504			Cornell Dubilier PM4P1	CAPACITOR, FIXED MYLAR, .1μf, 400vdc	1		
5-5	CR504			Motorola 10M10Z	DIODE	1		
5-6	CR505			Pacific Semi-Conductor 1N703	DIODE	1		
5-7	DS501-DS516			MEC 16-101	INDICATOR	16		
5-8	M501			MEC MN13	MAGNETIC CORE	1		
5-9	M502-M509			MEC MN11	MAGNETIC CORE	8		
5-10	N501			MEC TN130B	TRANSISTOR NETWORK	1		
5-11	N502-N517			MEC TN144	TRANSISTOR NETWORK	16		
5-12	P501			Cannon DD-50P	PLUG, Male, 50 pin contact, 5 amp rating	1		
5-13	R536			MIL RC20GF103K	RESISTOR, FIXED COMPOSITION, 10K, 10% 1/2W	1		
5-14	R502			MIL RC20GF182K	RESISTOR, FIXED COMPOSITION, 1.8K, 10% 1/2W	1		
5-15	R503-R534			MIL RC20GF562K	RESISTOR, FIXED COMPOSITION, 5.6K, 10% 1/2W	32		
5-16	R535			MIL RC20GF332K	RESISTOR, FIXED COMPOSITION, 3.3K, 10% 1/2W	1		
5-17	R537			MIL RC20GF391K	RESISTOR, FIXED COMPOSITION, 390 ohms, 10%, 1/2W	1		
5-18	R501			MIL RC20GF392K	RESISTOR, FIXED COMPOSITION, 3.9K, 10% 1/2W	1		
5-19	TJ501			Cannon DD-50S	CONNECTOR, Female, 50 pin contact, 5 amp rating	1		
5-20	XM501-XM509			JAN TS103P02	SOCKET, Tube, 9 Pin Miniature	9		
5-21	XN501-XN517			JAN TS101P01	SOCKET, Tube, Octal	17		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
6-1				MEC 72-6A	ASSEMBLY, TIMING LOGIC			
6-2	C608			MIL CM-30B-502K	CAPACITOR, FIXED MICA, 5000μμf, 10%, 500 vdc	1		
6-3	C609 C605 C617 C620			MIL CM-19B-102K	CAPACITOR, FIXED MICA, 1000μμf, 10%, 500 vdc	4		
6-4	C602			Cornell Dubilier PM4S47	CAPACITOR, FIXED MYLAR, .047μf, 400vdc	1		
6-5	C603 C604 C610			MIL CM-19B-471K	CAPACITOR, FIXED MICA, 470μμf, 10%, 500 vdc	3		
6-6	C615 C613			MIL CM-19B-272K	CAPACITOR, FIXED MICA, 2700μμf, 10%.500 vdc	2		
6-7	C618			Fansteel F110-1	CAPACITOR, (Blu Cap), 10μf, 25vdc	1		
6-8	C619			Fansteel F308-1	CAPACITOR, (Blu Cap), 100μf, 30vdc	1		
6-9	C601			Cornell Dubilier PM6S3	CAPACITOR, FIXED MYLAR, .03μf, 600vdc	1		
6-10	C606 C607 C611 C621			Cornell Dubilier PM4S1	CAPACITOR, FIXED MYLAR, .01μf, 400vdc	4		
6-11	CR601			Hoffman 1N703	DIODE, Zener	1		
6-12	CR602 CR604 CR605-CR607			Clevite CTP-503 or T12G	DIODE	5		
6-13	N601			MEC TN150	TRANSISTOR NETWORK	1		
6-14	N602 N611 N614			MEC TN138B	TRANSISTOR NETWORK	3		
6-15	N603 N606-N608			MEC TN90B	TRANSISTOR NETWORK	4		
6-16	N605 N609			MEC TN58	TRANSISTOR NETWORK	2		
6-17	N613			MEC TN111	TRANSISTOR NETWORK	1		
6-18	N604 N610			MEC TN28	TRANSISTOR NETWORK	2		
6-19	P601			Cannon DD-50P	PLUG, Male, 50 pin contact, 5 amp rating	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
6-20	R630 R628			MIL RC20GF104K	RESISTOR, FIXED COMPOSITION, 100K, 10% 1/2W	2		
6-21	R623 R629 R607 R608 R610 R614 R618 R619 R631			MIL RC20GF103K	RESISTOR, FIXED COMPOSITION, 10K, 10% 1/2W	9		
6-22	R602			MIL RC20GF153K	RESISTOR, FIXED COMPOSITION, 15K, 10% 1/2W	1		
6-23	R603			Allen Bradley JA1L040S253UC	POTENTIOMTER, 25K, 2W, Linear Taper	1		
6-24	R604 R617			MIL RC20GF223K	RESISTOR, FIXED COMPOSITION, 22K, 10% 1/2W	2		
6-25	R605 R606 R615 R625			MIL RC20GF332K	RESISTOR, FIXED COMPOSITION, 3.3K, 10% 1/2W	4		
6-26	R609			Allen Bradley JA1L040S252UC	POTENTIOMTER, 2W, Linear Taper, 2.5K	1		
6-27	R613 R626			MIL RC20GF152K	RESISTOR, FIXED COMPOSITION, 1500 ohms, 10%, 1/2W	2		
6-28	R612 R632			MIL RC20GF332K	RESISTOR, FIXED COMPOSITION, 33K, 10% 1/2W	2		
6-29	R615			MIL RC20GF562K	RESISTOR, FIXED COMPOSITION, 5.6K, 10% 1/2W	1		
6-30	R624 R627			MIL RC20GF102K	RESISTOR, FIXED COMPOSITION, 1000 ohms 10%, 1/2W	2		
6-31	TJ501			Cannon DD-50S	CONNECTOR, Female, 50 pin contact, 5 amp rating	1		
6-32	XN601- XN614			JAN TS101P01	SOCKET, Octal	14		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
7-1				MEC 72-7A	ASSEMBLY, POWER CONTROL	1		
7-2	CR701-CR709			G. E. IN1695	DIODE	9		
7-3	DS701-DS709			Eldema 1CG12-4535	LAMP, Neon to Spec. 21C-3864-7	9		
7-4	I701-I702			Eldema 1GF5-4976	LAMP, Incandescent, (Red)	2		
7-5	MV701			Beede E-25	METER, 1.2MA, (Scale 0-12) Horizontal Mounting.	1		
7-6	P701			Cannon DD-50P	PLUG	1		
7-7	R701			MIL RC20GF393K	RESISTOR, Fixed composition, 39K ±10% 1/2W	1		
7-8	R702			I. R. C. DCC	RESISTOR, Precision, 54K ±1% 1/2W	1		
7-9	R703			I. R. C. DCC	RESISTOR, Precision, 12K ±1% 1/2W	1		
7-10	R704			I. R. C. DCC	RESISTOR, Precision, 20K ±1% 1/2W	1		
7-11	R705			I. R. C. DCC	RESISTOR, Precision, 85K ±1% 1/2W	1		
7-12	R706, R707 R709-R722			MIL RC20GF104K	RESISTOR, Fixed composition, 100K ±10% 1/2W	16		
7-13	R708			I. R. C. DCC	RESISTOR, Precision, 250K ±1% 1/2W	1		
7-14	R723			MIL RC42GF820K	RESISTOR, Fixed composition, 82Ω ±10% 2W	1		
7-15	S701			Cutler Hammer ST52N	SWITCH, Toggle, DPDT	1		
7-16	S702			Oak 399655-MF	SWITCH, Rotary	1		
7-17	XDS701-XDS709			Eldema 11H-4593	INDICATOR HOLDER	9		
7-18				Whitso K-150	KNOB	1		
7-19				Eldema 11H-4110	LENS CAP, (Translucent)	1		
7-20				Eldema 11H-4119	LENS CAP, (Red)	8		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
1				McLean 2BB508C	ASSEMBLY, BROKER	1		
8-1				MEC 71-8A	ASSEMBLY, DATA LINE AMPLIFIER	1		
8-2	C801 C803			Cornell Dubilier PM4S1	CAPACITOR, Fixed Mylar, .01 uf, 400vdc	2		
8-3	C826 C827			Cornell Dubilier PM4S2	CAPACITOR, Fixed Mylar, .02uf, 400vdc	2		
8-4	C811-C814			Cornell Dubilier PM4P1	CAPACITOR, Fixed Mylar, .1uf, 400vdc	4		
8-5	C802 C837			Cornell Dubilier PM6D5	CAPACITOR, Fixed Mylar, .005uf, 600vdc	2		
8-6	C804 C805 C815			Cornell Dubilier PM2P47	CAPACITOR, Fixed Mylar, .47uf, 200vdc	3		
8-7	C824			Cornell Dubilier PM4S5	CAPACITOR, Fixed Mylar, .05uf, 400vdc	1		
8-8	C806			MIL CM-19B-501K	CAPACITOR, Fixed Mica, 500uuf, 10%, 500vdc	1		
8-9	C807 C809 C810			MIL CM-19B-202K	CAPACITOR, Fixed Mica, 2000uuf, 10%, 500vdc	3		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
8-10	C817- C819 C821 C825 C828			MIL CM-19B-101K	CAPACITOR, Fixed Mica, 100uf, 10%, 500vdc	6		
8-11	C816			MIL CM-19B-501K	CAPACITOR, Fixed Mica, 500uuf, 10%, 500vdc	1		
8-12	C820			MIL CM-19B-152K	CAPACITOR, Fixed Mica, 1500uuf, 10%, 500vdc	1		
8-13	C829- C831			MIL CM-19B-560K	CAPACITOR, Fixed Mica, 56uuf, 10%, 500vdc	3		
8-14	C808 C832 C833			Aerovox AEP8J	CAPACITOR, Fixed Plug-in, 40uf, 450V	3		
8-15	C834			Aerovox AEP88J	CAPACITOR, Fixed Plug-in, 40-40uf, 450vdc	1		
8-16	C822			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000uuf, 10%, 500vdc	1		
8-17	C823			MIL CM-19B-471K	CAPACITOR Fixed Mica, 470uuf, 10%, 500vdc	1		
8-18	CR801- CR804 CR809- CR815			Hughes HD6227	DIODE	11		
8-19	CR816- CR824			G E. 1N1695	DIODE	9		
8-20	CR805- CR808			Pacific Semiconductor PS030	DIODE	4		
8-21	F801			Bussmann AGC	FUSE, 1 Amp	1		
8-22	DS801- DS804			Eldema 1CC12-4535	LAMP, Neon to Spec. 21C-3864-7	4		
8-23	L801 L802			UTC MQA-12	INDUCTOR	2		
8-24	L803			UTC HVC-8	INDUCTOR	1		
8-25	P801			Cannon DD-50P	PLUG, Male, 50 Pin Contact, 5 Amp Rating	1		
8-26	R802			MIL RC20GF434J	RESISTOR, Fixed Composition, 430K, 5%, ½W	1		
8-27	R803 R809 R811 R820 R821			MIL RC20GF244J	RESISTOR, Fixed Composition, 240K, 5%, ½W	5		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
8-28	R805 R883 R823 R825 R826 R829 R831 R834- R837 R861 R866 R877 R880 R881 R854			MIL RC20GF104K	RESISTOR, Fixed Composition, 100K, 10%, ½W	17		
8-29	R806 R830 R859			MIL RC20GF563K	RESISTOR, Fixed Composition, 56K, 10%, ½W	3		
8-20	R807 R862 R865			MIL RC20GF124K	RESISTOR, Fixed Composition, 120K, 10%, ½W	3		
8-31	R815 R819			MIL RC20GF224K	RESISTOR, Fixed Composition, 220K, 10%, ½W	2		
8-32	R816			MIL RC20GF102K	RESISTOR, Fixed Composition, 1K, 10%, ½W	1		
8-33	R817 R818 R833 R868 R869 R871			MIL RC20GF623J	RESISTOR, Fixed Composition, 62K, 5%, ½W	6		
8-34	R828 R839 R845 R851			MIL RC20GF204J	RESISTOR, Fixed Composition, 200K, 5%, ½W	4		
8-35	R832 R838 R844 R850 R863 R864 R867 R870 R872			MIL RC20GF624J	RESISTOR, Fixed Composition, 620K, 5%, ½W	9		
8-36	R857			MIL RC20GF333K	RESISTOR, Fixed Composition, 33K, 10%, ½W	1		
8-37	R810			MIL RC20GF202J	RESISTOR, Fixed Composition, 2K, 5%, ½W	1		
8-38	R808 R856 R858			MIL RC20GF105K	RESISTOR, Fixed Composition, 1M, 10%, ½W	3		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
8-39	R827 R855			MIL RC20GF125K	RESISTOR, Fixed, Composition, 1.2M, 10%, ½W	2		
8-40	R860			MIL RC20GF222K	RESISTOR, FIXED, Composition, 2.2K, 10%, ½W	1		
8-41	R814			MIL RC42GF222K	RESISTOR, Fixed, Composition, 2.2K, 10%, 2W	1		
8-42	R840 R841 R846 R847 R852 R853			MIL RC42GF433J	RESISTOR, Fixed, Composition, 43K, 5%, 2W	6		
8-43	R842			MIL RC20GF205J	RESISTOR, Fixed, Composition, 2M, 5%, ½W	1		
8-44	R873 R874			MIL RC42GF101K	RESISTOR, Fixed, Composition, 100 ohms, 10%, 2W	2		
8-45	R879			MIL RC42GF511J	RESISTOR, Fixed, Composition, 510 ohms, 5%, 2W	1		
8-46	R875			Ward Leonard 10F8000	RESISTOR, Fixed, Wire Wound, 8K, 10W	1		
8-47	R878			Ward Leonard 10F3000	RESISTOR, FIXED, Wire Wound, 3K, 10W	1		
8-48	R876			MIL RC42GF202J	RESISTOR, Fixed, Composition, 2K, 5%, 2W	1		
8-49	R843 R849			Allen Bradley JA1L040S255UC	POTENTIOMETER, 2.5M, 2W, Linear Taper	2		
8-50	R822			Allen Bradley JA1L040S503UC	POTENTIOMETER, 50K, 2W, Linear Taper	1		
8-51	R801			Allen Bradley JA1L040S104UC	POTENTIOMETER, 100K, 2W, Linear Taper	1		
8-52	R804			MIL RC20GF271K	RESISTOR, Fixed, Composition, 270 ohms, 10%, ½W	1		
8-53	R812			MIL RC20GF432K	RESISTOR, Fixed, Composition, 4.3K, 10%, ½W	1		
8-54	R813			MIL RC20GF473K	RESISTOR, Fixed, Composition, 47K, 10%, ½W	1		
8-55	R848			MIL RC20GF105J	RESISTOR, Fixed, Composition, 1M, 5%, ½W	1		
8-56	R882			MIL RC20GF433K	RESISTOR, Fixed, Composition, 43K, 10%, ½W	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
8-57	T801			Triad J0-13	TRANSFORMER	1		
8-58	T802			Chicago Std. PHC-60	TRANSFORMER	1		
8-59	TJ801			Cannon DD-50S	CONNECTOR, Female, 50 Pin Contact, 5Amp Rating	1		
8-60	V801			Comm 6660	TUBE, Electron	1		
8-61	V802 V803 V805-V807			Comm 5963	TUBE, Electron	5		
8-62	V804 V808-V811			Comm 12AT7	TUBE, Electron	5		
8-63	V812 V815			Comm 0B2	TUBE, Electron	2		
8-64	V813 V814			Comm 0A2	TUBE, Electron	2		
8-65	XC808 XC832 XC833			JAN TS101P01	SOCKET, Octal, Mica Filled	3		
8-66	XDS801-XDS804			Eldema 11H4593	INDICATOR HOLDER	4		
8-67	XF801			Bussmann HKP	FUSE HOLDER	1		
8-68	XV802-XV811			JAN TS103P01	SOCKET, 9 Pin Miniature, Mica Filled	10		
8-69	XV801 XV812-XV815			JAN TS102P01	SOCKET, 7 Pin Miniature, Mica Filled	5		
8-70				JAN TS102U02	SHIELD, Tube	1		
8-71				JAN TS102U03	SHIELD, Tube	4		
8-72				JAN TS103U02	SHIELD, Tube	10		
8-73				Eldema 11H-4110	LENS CAP (Translucent)	3		
8-74				Eldema 11H-4119	LENS CAP (Red)	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
4-1				MEC 165-4C	ASSEMBLY, POWER SUPPLY	1		
4-2	C401 C402 C421-C423			Mallory 20-71937	CAPACITOR, Computer Grade, 4000μf 60 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	5		
4-3	C403 C425 C443 C444			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01μf 400 vdc	4		
4-4	C424			Cornell Dubilier PM4P1	CAPACITOR, Fixed, Mylar, .1μf 400 vdc	1		
4-5	C404 C426			Fansteel F308-1	CAPACITOR, Blu-cap, 100μf 30 vdc	2		
4-6	C441 C442			Mallory 20-71855	CAPACITOR, Computer Grade, 2000μf 100 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	2		
4-7	C445			Fansteel F316-1	CAPACITOR, Blu-cap, 30μf 100 vdc	1		
4-8	CR401 CR421			G.E. 4JA211AB1AC2	RECTIFIER	3		
4-9	CR402 CR422			International Rectifier IN1519	DIODE, Zener (1Z4.7)	2		
4-10	CR442			International Rectifier IN1524	DIODE, Zener (1Z12)	1		
4-11	F401 F403			Bussmann AGC	FUSE, 1 Amp	2		
4-12	F402			Bussmann AGC	FUSE, 3 Amp	1		
4-13	F404			Bussmann MDX	FUSE, Fusetron, Slo-Blow, 3 Amp.	1		
4-14	P401			Cannon DD-50P	PLUG	1		
4-15	Q423 Q442			Delco 2N558	TRANSISTOR, (Mount with Parts #100 & #101)	2		
4-16	Q401 Q421 Q441 Q422			Delco 2N443	TRANSISTOR, (Lug type Leads)	4		
4-17	Q402 Q403 Q424 Q443			G.E. 2N525	TRANSISTOR	4		
4-18	Q404 Q425 Q444			Sylvan'a 2N377A	TRANSISTOR	3		
4-19	R401, R402 R421A R421B R441 R442			Ward Leonard 5X1	RESISTOR, Axiohm, 1Ω 5W	6		
4-20	R403 R443			Ward Leonard 5X2	RESISTOR, Axiohm, 2Ω 5W	2		
4-21	R404 R425 R444			MIL RC42GF102K	RESISTOR, Fixed composition, 1K ±10% 2W	3		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
4-22	R405			MIL RC42GF151K	RESISTOR, Fixed composition, 150Ω ±10% 2W	1		
4-23	R406			MIL RC20GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1/2W	1		
4-24	R407 R428 R447			MIL RC20GF101K	RESISTOR, Fixed composition, 100Ω ±10% 1/2W	3		
4-25	R408			MIL RC20GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1/2W	1		
4-26	R409 R430 R449			MIL RC20GF822K	RESISTOR, Fixed composition, 8.2K ±10% 1/2W	3		
4-27	R410 R431 R450			MIL RC20GF621J	RESISTOR, Fixed composition, 620Ω ±5% 1/2W	3		
4-28	R411 R432			MIL RC20GF472K	RESISTOR, Fixed composition, 4.7K ±10% 1/2W	2		
4-29	R412			MIL RC32GF121K	RESISTOR, Fixed composition, 120Ω ±10% 1W	1		
4-30	R414 R435			Chicago Tel. RA20LASB250A	POTENTIOMETER, 25Ω 2W	2		
4-31	R415			MIL RC32GF820J	RESISTOR, Fixed composition, 82Ω ±5% 1W	1		
4-32	R413			MIL RC42GF131J	RESISTOR, Fixed composition, 130Ω ±5% 2W	1		
4-33	R422			Ward Leonard 10F1	RESISTOR, Fixed, Wire wound, 1Ω 10W	1		
4-34	R423 R424			Ward Leonard 10F2	RESISTOR, Fixed, Wire wound, 2Ω 10W	2		
4-35	R426 R437			Ward Leonard 10F150	RESISTOR, Fixed, Wire wound, 150Ω 10W	2		
4-36	R427 R446			MIL RC32GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1W	2		
4-37	R429 R448			MIL RC32GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1W	2		
4-38	R433 R416			MIL RC42GF271K	RESISTOR, Fixed composition, 270Ω ±10% 2W	2		
4-39	R436			MIL RC32GF510J	RESISTOR, Fixed composition, 51Ω ±5% 1W	1		
4-40	R434			MIL RC42GF181J	RESISTOR, Fixed composition, 180Ω ±5% 2W	1		
4-41	R451			MIL RC42GF302J	RESISTOR, Fixed composition, 3K ±5% 2W	1		
4-42	R453			Allen Bradley JLU-1011 or JA1L040S101UC	POTENTIOMETER, 100Ω 2W, Linear Taper	1		
4-43	R454			MIL RC42GF272J	RESISTOR, Fixed composition, 2.7K ±5% 2W	1		
4-44	R455			Ward Leonard 5X500	RESISTOR, Fixed, Axiohm, 500Ω 5W	1		
4-45	R452			MIL RC32GF561J	RESISTOR, Fixed composition, 560Ω ±5% 1W	1		
4-46	R445			Ward Leonard 10F250	RESISTOR, Fixed, Wire wound, 250Ω 10W	1		
4-47	T401			TTI 5486	TRANSFORMER	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
4-48	TJ401-TJ404			H.H. Smith 221	JACK, Midget Banana (Black)	4		
4-49	XF401-XF404			Bussmann HKP	FUSEHOLDER	4		

CHAPTER VIII

WIRE LIST

INDEX

WIRE NO.	REFERENCE	PAGE	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	J1	8-13		DLA #1A		
	J2	8-14		DLA #1B		
	J3	8-15		DLA #2A		
	J4	8-16		DLA #2B		
	J5	8-17		Control #1		
	J5A	8-18		Control #1		
	J6	8-19		Control #2		
	J6A	8-20		Control #2		
	J7	8-21		Buffer #1A		
	J8	8-22		Buffer #1B		
	J9	8-23		Buffer #2A		
	J10	8-24		Buffer #2B		
	J11	8-25		Output Register 1A		
	J12	8-26		Output Register 1B		
	J13	8-27		Output Register 2A		
	J14	8-28		Output Register 2B		
	J15	8-29		Timing Logic 1A		
	J16	8-30		Timing Logic 1B		
	J17	8-31		Timing Logic 2A		
	J18	8-32		Timing Logic 2B		
	J19	8-33		Power Control		

NOTES:

INDEX

WIRE NO.	REFERENCE	PAGE	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	J20	8-9		Output Signal Connector		
	J21	8-10		Output Signal Connector		
	J22	8-11		Output Signal Connector		
	J23	8-12		Output Signal Connector		
	J31	8-34		Power Supply A		
	J32	8-35		Power Supply B		
	J33	8-4		Power Connector		
	J34	8-5		Input Signal Connector		
	J35	8-5		Input Signal Connector		
	J36	8-6		Input Signal Connector		
	J37	8-6		Input Signal Connector		
	J38	8-7		Input Signal Connector		
	J39	8-7		Input Signal Connector		
	J40	8-8		Input Signal Connector		
	J41	8-8		Input Signal Connector		
	J42	8-47		Recorder Connector		

NOTES:

INDEX

WIRE NO.	REFERENCE	PAGE	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	+12V (A)	8-37				
	0V (A)	8-37				
	-20V (A)	8-38				
	-85V (A)	8-39				
	+12V (B)	8-40				
	0V (B)	8-40				
	-20V (B)	8-41				
	-85V (B)	8-42				
	AC Switched	8-43				
	AC Common	8-43				
	SW1	8-44				
	I1	8-44				
	F1	8-45				
	F2	8-45				
	TB1	8-46				
	BL1	8-46				

NOTES:

J33

* POWER CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	SW1-2	1	AC (Hot)	14	S
	B	SW1-5	1	AC (Common)	14	W
	C					
	D					
	E	Frame		Frame Ground	14	BK

NOTES:
* MS3102A-18-11P

Rev. 6/15/61

J34

Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-15	2	Data Shield tied to chassis ground through connector.	RG174/U	

NOTES:

J35

Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-17	2	Data Shield tied to chassis ground through connector.	RG174/U	

NOTES:

J36
Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J2-15	2	Data	RG174/U	
				Shield tied to chassis ground through connector.		

NOTES:

J37
Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J2-17	2	Data	RG174/U	
				Shield tied to chassis ground through connector.		

NOTES:

J38

Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-15	2	Data	RG174/U	
				Shield tied to chassis ground through connector.		

NOTES:

J39

Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-17	2	Data	RG174/U	
				Shield tied to chassis ground through connector.		

NOTES:

J40

Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J4-15	2	Data	RG174/U	
				Shield tied to chassis ground through connector.		

NOTES:

J41

Input Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J4-17	2	Data	RG174/U	
				Shield tied to chassis ground through connector.		

NOTES:

J20
Output Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J5-26	2	Sample Pulse 1A	22	BR
	B					
	C	J11-33	2	DL 1A1	22	BR
	D					
	E	J11-31	2	DL 1A2	22	O
	F					
	G	J11-29	2	DL 1A3	22	Y
	H	J11-27	2	DL 1A4	22	G
	I	J11-25	2	DL 1A5	22	BL
	J					
	K	J11-23	2	DL 1A6	22	BR
	L	J11-21	2	DL 1A7	22	O
	M					
	N	J11-19	2	DL 1A8	22	Y
	O	0V(A)-19	2	Sig. Gnd.	14	B
	P	J12-33	2	DL 1A9	22	BL
	R					
	S					
	T	J12-31	2	DL 1A10	22	BR
	U					
	V	J12-29	2	DL 1A11	22	O
	W					
	X	J12-27	2	DL 1A12	22	Y
	Y					
	Z					

NOTES: MS3102A-32-7P

J20
Output
Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	a	J12-25	2	DL 1A13	22	G
	b					
	c	J12-23	2	DL 1A14	22	BL
	d					
	e	J12-21	2	DL 1A15	22	BR
	f	J12-19	2	DL 1A16	22	O
	g	J5-32	2	EOM 1A	22	Y
	h					
	j					
	k					

NOTES: MS3102A-32-7P

J21
Output Signal
Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J6-26	2	Sample Pulse 2A	22	W/BR
	B					
	C	J13-33	2	DL 2A1	22	BR
	D					
	E	J13-31	2	DL 2A2	22	O
	F					
	G	J13-29	2	DL 2A3	22	Y
	H	J13-27	2	DL 2A4	22	G
	I	J13-25	2	DL 2A5	22	BL
	J					
	K	J13-23	2	DL 2A6	22	BR
	L	J13-21	2	DL 2A7	22	O
	M					
	N	J13-19	2	DL 2A8	22	Y
	O					
	P	J14-33	2	DL 2A9	22	BL
	R					
	S					
	T	J14-31	2	DL 2A10	22	BR
	U					
	V	J14-29	2	DL 2A11	22	O
	W					
	X	J14-27	2	DL 2A12	22	Y
	Y					
	Z					

NOTES:
MS3102A-32-7P

J21
Output Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	a	J14-25	2	DL 2A13	22	G
	b					
	c	J14-23	2	DL 2A14	22	BL
	d					
	e	J14-21	2	DL 2A15	22	BR
	f	J14-19	2	DL 2A16	22	O
	g	J6-32	2	EOM 2A	22	W/Y
	h					
	j					
	k					

NOTES:
MS3102-32-7P

J22
Output Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J5-28	2	Sample Pulse 1B	22	O
	B					
	C	J11-32	2	DL 1B1	22	W/BR
	D					
	E	J11-30	2	DL 1B2	22	W/O
	F					
	G	J11-28	2	DL 1B3	22	W/Y
	H	J11-26	2	DL 1B4	22	W/G
	I	J11-24	2	DL 1B5	22	W/BL
	J					
	K	J11-22	2	DL 1B6	22	W/BR
	L	J11-20	2	DL 1B7	22	W/O
	M					
	N	J11-18	2	DL 1B8	22	W/Y
	O					
	P	J12-32	2	DL 1B9	22	W/BL
	R					
	S					
	T	J12-30	2	DL 1B10	22	W/BR
	U					
	V	J12-28	2	D1 1B11	22	W/O
	W					
	X	J12-26	2	DL 1B12	22	W/Y
	Y					
	Z					

NOTES: MS3102A-32-7P

J22
Output Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	a	J12-24	2	DL 1B13	22	W/G
	b					
	c	J12-22	2	DL 1B14	22	W/BL
	d					
	e	J12-20	2	DL 1B15	22	W/BR
	f	J12-18	2	DL 1B16	22	W/O
	g	J5-33	2	EOM 1B	22	W/Y
	h					
	j					
	k					

NOTES: MS3102A-32-7P

J23
Output Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J6-28	2	Sample Pulse 2B	22	W/G
	B					
	C	J13-32	2	DL 2B1	22	W/BR
	D					
	E	J13-30	2	DL 2B2	22	W/O
	F					
	G	J13-28	2	DL 2B3	22	W/Y
	H	J13-26	2	DL 2B4	22	W/G
	I	J13-24	2	DL 2B5	22	W/BL
	J					
	K	J13-22	2	DL 2B6	22	W/BR
	L	J13-20	2	DL 2B7	22	W/O
	M					
	N	J13-18	2	DL 2B8	22	W/Y
	O					
	P	J14-32	2	DL 2B9	22	W/BL
	R					
	S					
	T	J14-30	2	DL 2B10	22	W/BR
	U					
	V	J14-28	2	DL 2B11	22	W/O
	W					
	X	J14-26	2	DL 2B12	22	W/Y
	Y					
	Z					

NOTES:
MS3102A-32-7P

J23
Output Signal Connector

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	a	J14-24	2	DL 2B13	22	W/G
	b					
	c	J14-22	2	DL 2B14	22	W/BL
	d					
	e	J14-20	2	DL 2B15	22	W/BR
	f	J14-18	2	DL 2B16	22	W/O
	g	J6-33	2	EOM 2B	22	Y
	h					
	j					
	k					

NOTES:
MS3102A-32-7P

J1
DLA #1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J5-1	2	Clock 1A (1KC)	22	BR
	8					
	9	J5-7	2	EOW 1A	22	O
	10					
	11	J5-5	2	SOW 1A	22	Y
	12					
	13	J5-3	2	Data 1A	22	G
	14					
	15	J34-1	2	Data	RG174/U	
	16					
	17	J35-1	2	Data	RG174/U	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J1
DLA #1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	AC(Hot)-4	1	AC Switched	20	W/S
	35					
	36	AC(Common)-4	1	AC Common	20	W
	37					
	38	J19-23	1	-250V (1A)	22	W/V
	39	J19-18	1	+250V (1A)	22	W/R
	40					
	41					
	42					
	43					
	44					
	45	0V(A)-1	1	0V (A)	20	BK
	46	0V(A)-1	1	0V (A)	20	BK
	47					
	48					
	49	J42-A	2	To Tape Recorder	RG174/U	
	50	Frame		Chassis Gnd.	20	BK

NOTES:

J2
DLA #1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J5-2	2	Clock 1B (1KC)	22	W/BR
	8					
	9	J5-8	2	EOW 1B	22	W/O
	10					
	11	J5-6	2	SOW 1B	22	W/Y
	12					
	13	J5-4	2	Data 1B	22	W/G
	14					
	15	J36-1	2	Data	RG174/U	
	16					
	17	J37-1	2	Data	RG174/U	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J2
DLA #1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	AC(Hot)-5	1	AC Switched	20	W/S
	35					
	36	AC(Common)-5	1	AC Common	20	W
	37					
	38	J19-24	1	+250V (1B)	22	W/V
	39	J19-19	1	+250V (1B)	22	W/R
	40					
	41					
	42					
	43					
	44					
	45	0V (B)-2	1	0V (B)	20	BK
	46	0V (B)-2	1	0V (B)	20	BK
	47					
	48					
	49	J42-B	2	To Tape Recorder	RG174/U	
	50	Frame		Chassis Gnd	20	BK

NOTES:

J3

DLA #2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J6-1	2	Clock 2A (1KC)	22	BR
	8					
	9	J6-7	2	EOW 2A	22	O
	10					
	11	J6-5	2	SOW 2A	22	Y
	12					
	13	J6-3	2	Data 2A	22	G
	14					
	15	J38-1	2	Data	RG174/U	
	16					
	17	J39-1	2	Data	RG174/U	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J3

DLA #2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	AC(Hot)-6	1	AC Switched	20	W/S
	35					
	36	AC(Common)-6	1	AC Common	20	W
	37					
	38	J19-25	1	-250V (2A)	22	W/V
	39	J19-20	1	+250V (2A)	22	W/R
	40					
	41					
	42					
	43					
	44					
	45	0V (A)	1	0V (A)	20	BK
	46	0V (A)	1	0V (A)	20	BK
	47					
	48					
	49	J42-C	2	To Tape Recorder	RG174/U	
	50	Frame		Chassis Gnd	20	BK

NOTES:

J4

DLA #2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J6-2	2	Clock 2B (1KC)	22	W/BR
	8					
	9	J6-8	2	EOW 2B	22	W/O
	10					
	11	J6-6	2	SOW 2B	22	W/Y
	12					
	13	J6-4	2	Data 2B	22	W/G
	14					
	15	J40-1	2	Data	RG174/U	
	16					
	17	J41-1	2	Data	RG174/U	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J4

DLA #2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	AC(Hot)-7	1	AC Switched	20	W/S
	35					
	36	AC(Common)-7	1	AC Common	20	W
	37					
	38	J19-26	1	-250V (2B)	22	W/V
	39	J19-21	1	+250V (2B)	22	W/R
	40					
	41					
	42					
	43					
	44					
	45	0V (B)-4	1	0V (B)	20	BK
	46	0V (B)-4	1	0V (B)	20	BK
	47					
	48					
	49	J42-D	2	To Tape Recorder	RG174/U	
	50	Frame		Chassis Gnd	20	BK

NOTES:

J5
Control #1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-7	2	Clock 1A (1KC)	22	BR
	2	J2-7	2	Clock 1B (1KC)	22	W/BR
	3	J1-13	2	Data 1A	22	G
	4	J2-13	2	Data 1B	22	W/G
	5	J1-11	2	SOW1A	22	Y
	6	J2-11	2	SOW1B	22	W/Y
	7	J1-9	2	EOW1A	22	O
	8	J2-9	2	EOW1B	22	W/O
	9	J15-4	2	8:1 Counter Gate	22	BL
	10	J15-8	2	Sample Pulse Gate A	22	BR
	11	J16-8	2	Sample Pulse Gate B	22	O
	12					
	13					
	14					
	15	J7-8	2	(A) EOW F.F.	22	BL
	16	J8-8	2	(B) EOW F.F.	22	W/BL
	17					
	18	J16-1	2	Clock (B)	22	W/O
	19	J15-1	2	Clock (A)	22	W/BR
	20	J16-12	2	Data (B)	22	W/Y
	21	J15-12	2	Data (A)	22	W/G
	22	J16-11	2	SOW (B)	22	BR
	23	J15-11	2	SOW (A)	22	O
	24	J8-6	2	EOW (B)	22	Y
	25	J7-6	2	EOW (A)	22	G

NOTES:

J5
Control #1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J20-A	2	Sample Pulse (1A)	22	BR
	27	J15-7	2	Sample Pulse (1A)	22	Y
	28	J22-A	2	Sample Pulse (1B)	22	O
	29	J16-7	2	Sample Pulse (1B)	22	G
	30	J15-16	2	SOW	22	BL
	31	J16-16	2	SOW	22	W/BR
	32	J20-g	2	EOM 1A	22	Y
	33	J22-g	2	EOM 1B	22	W/Y
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J11-42	1	-10V (A)	20	V
	43					
	44	+12V (A)-5	1	+12V (A)	20	R
	45	0V (A)-5	1	0V (A)	20	BK
	46	0V (A)-5	1	0V (A)	20	BK
	47	-20V (A)-5	1	-20V (A)	20	S
	48	-20V (A)-5	1	-20V (A)	20	S
	49	-85 (A)-5	1	-85V (A)	22	W/BK
	50	Frame		Chassis Gnd.	20	BK

NOTES:

J5A
Control #1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	AC(hot)-10	1	AC Switched	22	W/S
	2					
	3	AC(Common)11	1	AC Common	22	W
	4					
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J5A
Control #1

TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
26					
27					
28					
29					
30					
31					
32					
33					
34					
35					
36					
37					
38					
39					
40					
41					
42	J12-42	1	-10V (B)	22	V
43					
44	+12V(B)-5	1	+12V (B)	22	R
45	0V(B)-5	1	0V (B)	22	BK
46					
47	-20V (B)-5	1	-20V (B)	22	S
48					
49					
50					

TES:

J6
Control #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-7	2	Clock 2A (1KC)	22	BR
	2	J4-7	2	Clock 2B (1KC)	22	W/BR
	3	J3-13	2	Data 2A	22	G
	4	J4-13	2	Data 2B	22	W/GR
	5	J3-11	2	SOW2A	22	Y
	6	J4-11	2	SOW2B	22	W/Y
	7	J3-9	2	EOW2A	22	O
	8	J4-9	2	EOW2B	22	W/O
	9	J18-4	2	8:1 Counter Gate	22	W/BL
	10	J17-8	2	Sample Pulse Gate A	22	BR
	11	J18-8	2	Sample Pulse Gate B	22	O
	12					
	13					
	14					
	15	J9-8	2	(A) EOW FF	22	BL
	16	J10-8	2	(B) EOW FF	22	W/BL
	17					
	18	J18-1	2	Clock (B)	22	W/BR
	19	J17-1	2	Clock (A)	22	W/O
	20	J18-12	2	Data (B)	22	W/Y
	21	J17-12	2	Data (A)	22	W/G
	22	J18-11	2	SOW (B)	22	BR
	23	J17-11	2	SOW (A)	22	O
	24	J10-6	2	EOW (B)	22	Y
	25	J9-6	2	EOW (A)	22	G

NOTES:

J6
Control #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J21-A	2	Sample Pulse (2A)	22	W/BR
	27	J17-7	2	Sample Pulse (2A)	22	BL
	28	J23-A	2	Sample Pulse (2B)	22	W/G
	29	J18-7	2	Sample Pulse (2B)	22	G
	30	J17-16	2	SOW	22	O
	31	J18-16	2	SOW	22	W/O
	32	J21-g	2	EOM 2A	22	W/Y
	33	J23-g	2	EOM 2B	22	Y
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J14-42	1	-10V (B)	20	V
	43					
	44	+12V(B)-6	1	+12V (B)	20	R
	45	0V(B)-6	1	0V (B)	20	BK
	46	0V(B)-6	1	0V (B)	20	BK
	47	-20V(B)-6	1	-20V (B)	20	S
	48	-20V(B)-6	1	-20V (B)	20	S
	49	-85V(B)-6	1	-85V (B)	22	W/BK
	50	Frame		Chassis Gnd.	20	BK

NOTES:

J6A
Control #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	AC(Hot)-11	1	AC Switched	22	W/S
	2					
	3	AC(Common)-12	1	AC Common	22	W
	4					
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J6A
Control #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J13-42	1	-10V (A)	22	V
	43					
	44	+12V(A)-6	1	+12V (A)	22	R
	45	0V (A)-6	1	0V (A)	22	BK
	46					
	47	-20V(A)-6	1	-20V (A)	22	S
	48					
	49					
	50					

NOTES:

J7
Buffer 1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J15-10	2	Data	22	BR
	2	J15-2	2	Clock Ø2	22	O
	3	J15-15	2	SOW	22	Y
	4	J11-1	2	Data	22	W/G
	5	J15-6	2	SOW	22	W/O
	6	J5-25	2	EOW	22	G
	7	J15-9	2	Sample Pulse Gate	22	W/Y
	8	J5-15	2	A EOW F.F.	22	BL
	9	J15-18	2	EOW	22	BR
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24	J8-42	2	EOW to Paired Receiver	22	G
	25					

NOTES:

J7
Buffer 1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J8-24	1	EOW from Paired Receiver	22	G
	43					
	44	+12V(A)-7	1	+12V (A)	20	R
	45	0V(A)-7	1	0V (A)	20	BK
	46	0V(A)-7	1	0V (A)	20	BK
	47	-20V(A)-7	1	-20V (A)	20	S
	48	-20V(A)-7	1	-20V (A)	20	S
	49					
	50	Rack		Chassis Gnd	20	BK

NOTES:

J8

Buffer - 1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J16-10	2	Data	22	W/BR
	2	J16-2	2	Clock Ø 2	22	W/G
	3	J16-15	2	SOW	22	O
	4	J12-1	2	Data	22	BL
	5	J16-6	2	SOW	22	BR
	6	J5-24	2	EOW	22	Y
	7	J16-9	2	Sample Pulse Gate	22	W/O
	8	J5-16	2	A EOW F.F.	22	W/BL
	9	J16-18	2	EOW	22	G
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24	J7-42	2	EOW to Paired Receiver	22	G
	25					

NOTES:

J8

BUFFER- 1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J7-24	1	EOW from Paired Receiver	22	G
	43					
	44	+12V(B)-8	1	+12 (B)	20	R
	45	0V (B)-8	1	0V (B)	20	BK
	46	0V (B)-8	1	0V (B)	20	BK
	47	-20V (B)-8	1	-20V (B)	20	S
	48	-20V(B)-8	1	-20V (B)	20	S
	49					
	50	Rack		Chassis Gnd	20	BK

NOTES:

J9

Buffer 2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J17-10	2	Data	22	BR
	2	J17-2	2	Clock Ø 2	22	O
	3	J17-15	2	SOW	22	W/Y
	4	J13-1	2	Data	22	W/G
	5	J17-6	2	SOW	22	W/BL
	6	J6-25	2	EOW	22	G
	7	J17-9	2	Sample Pulse Gate	22	W/BR
	8	J6-15	2	(A) EOW F.F.	22	BL
	9	J17-18	2	EOW	22	W/O
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24	J10-42	2	EOW to Paired Receiver	22	G
	25					

NOTES:

J9

Buffer 2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J10-24	1	EOW from Paired Receiver	22	G
	43					
	44	+12V(A)-9	1	+12V (A)	20	R
	45	0V(A)-9	1	0V (A)	20	BK
	46	0V (A)-9	1	0V (A)	20	BK
	47	-20V(A)-9	1	-20V (A)	20	S
	48	-20V(A)-9	1	-20V (A)	20	S
	49					
	50	Rack		Chassis Gnd	20	BK

NOTES:

J10

Buffer 2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J18-10	2	Data	22	W/BR
	2	J18-2	2	Clock Ø 2	22	W/G
	3	J18-15	2	SOW	22	O
	4	J14-1	2	Data	22	BR
	5	J18-6	2	SOW	22	W/O
	6	J6-24	2	EOW (B)	22	Y
	7	J18-9	2	Sample Pulse Gate	22	BL
	8	J6-16	2	(B) EOWFF	22	W/BL
	9	J18-18	2	EOW	22	G
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24	J9-42	2	EOW to Paired Receiver	22	G
	25					

NOTES:

J10

Buffer 2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J9-24	1	EOW from Paired Receiver	22	G
	43					
	44	+12V(B)-10	1	+12V (B)	20	R
	45	0V(B)-10	1	0V (B)	20	BK
	46	0V(B)-10	1	0V (B)	20	BK
	47	-20V(B)-10	1	-20V (B)	20	S
	48	-20V(B)-10	1	-20V (B)	20	S
	49					
	50	Rack		Chassis Gnd	20	BK

NOTES:

J11
Output Register 1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J7-4	2	Data	22	W/G
	2	J15-17	2	S. R. Gate	22	W/BR
	3	J15-3	2	Clock Ø 2	22	G
	4	J15-14	2	Reset	22	BL
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18	J22-N	2	Data Line 1B8	22	W/Y
	19	J20-N	2	Data Line 1A8	22	Y
	20	J22-L	2	Data Line 1B7	22	W/O
	21	J20-L	2	Data Line 1A7	22	O
	22	J22-K	2	Data Line 1B6	22	W/BR
	23	J20-K	2	Data Line 1A6	22	BR
	24	J22-I	2	Data Line 1B5	22	W/BL
	25	J20-I	2	Data Line 1A5	22	BL

NOTES:

J11
Output Register 1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J22-H	2	Data Line 1B4	22	W/G
	27	J20-H	2	Data Line 1A4	22	G
	28	J22-G	2	Data Line 1B3	22	W/Y
	29	J20-G	2	Data Line 1A3	22	Y
	30	J22-E	2	Data Line 1B2	22	W/O
	31	J20-E	2	Data Line 1A2	22	O
	32	J22-C	2	Data Line 1B1	22	W/BR
	33	J20-C	2	Data Line 1A1	22	BR
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J5-42	1	-10V (A)	20	V
	43					
	44	+12V(A)-11	1	+12V (A)	20	R
	45	0V(A)-11	1	0V (A)	20	BK
	46	0V(A)-11	1	0V (A)	20	BK
	47	-20V(A)-11	1	-20V	20	S
	48	-20V(A)-11	1	-20V	20	S
	49	-85V(A)-11	1	-85V	22	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J12

Output Register 1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J8-4	2	Data	22	BL
	2	J16-17	2	S.R. Gate	22	W/BL
	3	J16-3	2	Clock ∅ 2	22	G
	4	J16-14	2	Reset	22	W/O
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18	J22-f	2	Data Line 1B16	22	W/O
	19	J20-f	2	Data Line 1A16	22	O
	20	J22-e	2	Data Line 1B15	22	W/BR
	21	J20-e	2	Data Line 1B15	22	BR
	22	J22-c	2	Data Line 1B14	22	W/BL
	23	J20-c	2	Data Line 1A14	22	BL
	24	J22-a	2	Data Line 1B13	22	W/G
	25	J20-a	2	Data Line 1A13	22	G

NOTES:

J12

Output Register 1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J22-X	2	Data Line 1B12	22	W/Y
	27	J20-X	2	Data Line 1A12	22	Y
	28	J22-V	2	Data Line 1B11	22	W/O
	29	J20-V	2	Data Line 1A11	22	O
	30	J22-T	2	Data Line 1B10	22	W/BR
	31	J20-T	2	Data Line 1A10	22	BR
	32	J22-P	2	Data Line 1B9	22	W/BL
	33	J20-P	2	Data Line 1A9	22	BL
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J5A-42	1	-10V (B)	22	V
	43					
	44	+12V(B)-12	1	+12V (B)	20	R
	45	0V(B)-12	1	0V (B)	20	BK
	46	0V(B)-12	1	0V (B)	20	BK
	47	-20V(B)-12	1	-20V (B)	20	S
	48	-20V(B)-12	1	-20V (B)	20	S
	49	-85V(B)-12	1	-85V (B)	22	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J13

Output Register 2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J9-4	2	Data	22	W/G
	2	J17-17	2	S.R. Gate	22	W/BL
	3	J17-3	2	Clock Ø 2	22	BR
	4	J17-14	2	Reset	22	G
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18	J23-N	2	Data Line 2B8	22	W/Y
	19	J21-N	2	Data Line 2A8	22	Y
	20	J23-L	2	Data Line 2B7	22	W/O
	21	J21-L	2	Data Line 2A7	22	O
	22	J23-K	2	Data Line 2B6	22	W/BR
	23	J21-K	2	Data Line 2A6	22	BR
	24	J23-I	2	Data Line 2B5	22	W/BL
	25	J21-I	2	Data Line 2A5	22	BL

NOTES:

J13

Output Register 2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J23-H	2	Data Line 2B4	22	W/G
	27	J21-H	2	Data Line 2A4	22	G
	28	J23-G	2	Data Line 2B3	22	W/Y
	29	J21-G	2	Data Line 2A3	22	Y
	30	J23-E	2	Data Line 2B2	22	W/O
	31	J21-E	2	Data Line 2A2	22	O
	32	J23-C	2	Data Line 2B1	22	W/BR
	33	J21-C	2	Data Line 2A1	22	BR
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J6A-42	1	+10V (A)	22	V
	43					
	44	+12V(A)-13	1	+12V (A)	20	R
	45	0V(A)-13	1	0V (A)	20	BK
	46	0V(A)-13	1	0V (A)	20	BK
	47	-20V(A)-13	1	-20V (A)	20	S
	48	-20V(A)-13	1	-20V (A)	20	S
	49	-85V(A)-13	1	-85V (A)	22	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J14
Output Register 2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J10-4	2	Data	22	BR
	2	J18-17	2	S.R. Gate	22	BL
	3	J18-3	2	Clock ø 2	22	Y
	4	J18-14	2	Reset	22	W/G
	5					
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18	J23-f	2	Data Line 2B16	22	W/O
	19	J21-f	2	Data Line 2A16	22	O
	20	J23-e	2	Data Line 2B15	22	W/BR
	21	J21-e	2	Data Line 2A15	22	BR
	22	J23-c	2	Data Line 2B14	22	W/BL
	23	J21-c	2	Data Line 2A14	22	BL
	24	J23-a	2	Data Line 2B13	22	W/G
	25	J21-a	2	Data Line 2A13	22	G

NOTES:

J14
Output Register 2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J23-X	2	Data Line 2B12	22	W/Y
	27	J21-X	2	Data Line 2A12	22	Y
	28	J23-V	2	Data Line 2B11	22	W/O
	29	J21-V	2	Data Line 2A11	22	O
	30	J23-T	2	Data Line 2B10	22	W/BR
	31	J21-T	2	Data Line 2A10	22	BR
	32	J23-P	2	Data Line 2B9	22	W/BL
	33	J21-P	2	Data Line 2A9	22	BL
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42	J6-42	1	-10V (B)	20	V
	43					
	44	+12V(B)-14	1	+12V (B)	20	R
	45	0V(B)-14	1	0V (B)	20	BK
	46	0V(B)-14	1	0V (B)	20	BK
	47	-20V(B)-14	1	-20V (B)	20	S
	48	-20V(B)-14	1	-20V (B)	20	S
	49	-85V (B)-14	1	-85V (B)	20	W/BK
	50	Frame		Chassis Gnd		BK

NOTES:

J15
Timing Logic 1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-19	2	Clock A	22	W/BR
	2	J7-2	2	Clock Ø 2	22	O
	3	J11-3	2	Clock Ø 2	22	G
	4	J5-9	2	8:1 Counter Gate	22	BL
	5					
	6	J7-5	2	SOW	22	W/O
	7	J5-27	2	Sample Pulse (1A)	22	V
	8	J5-10	2	Sample Pulse Gate	22	BR
	9	J7-7	2	Sample Pulse Gate	22	W/Y
	10	J7-1	2	Data	22	BR
	11	J5-23	2	SOW A	22	O
	12	J5-21	2	Data	22	W/G
	13					
	14	J11-4	2	Reset	22	BL
	15	J7-3	2	SOW	22	Y
	16	J5-30	2	SOW	22	BL
	17	J11-2	2	S. R. Gate	22	W/BR
	18	J7-9	2	EOW	22	BR
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J15
Timing Logic 1A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V(A)-15	1	+12V (A)	20	R
	45	0V(A)-15	1	0V (A)	20	BK
	46	0V(A)-15	1	0V (A)	20	BK
	47	-20V(A)-15	1	-20V (A)	20	S
	48	-20V(A)-15	1	-20V (A)	20	S
	49					
	50	Frame		Chassis Gnd	20	BK

NOTES:

J16

Timing Logic 1 B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-18	2	Clock B	22	W/O
	2	J8-2	2	Clock Ø 2	22	W/G
	3	J12-3	2	Clock Ø 2	22	G
	4			8:1 Counter Gate		
	5					
	6	J8-5	2	SOW	22	BR
	7	J5-29	2	Sample Pulse (1B)	22	G
	8	J5-11	2	Sample Pulse Gate	22	O
	9	J8-7	2	Sample Pulse Gate	22	W/O
	10	J8-1	2	Data	22	W/BR
	11	J5-22	2	SOW (B)	22	BR
	12	J5-20	2	Data	22	W/Y
	13					
	14	J12-4	2	Reset	22	W/O
	15	J8-3	2	SOW	22	O
	16	J5-31	2	SOW	22	W/BR
	17	J12-2	2	S.R. Gate	22	W/BL
	18	J8-9	2	EOW	22	G
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J16

Timing Logic 1B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V(B)-16	1	+12V (B)	20	R
	45	0V(B)-16	1	0V (B)	20	BK
	46	0V(B)-16	1	0V (B)	20	BK
	47	-20V(B)-16	1	-20V (B)	20	S
	48	-20V(B)-16	1	-20V (B)	20	S
	49					
	50	Frame		Chassis Gnd	20	BK

NOTES:

J17

Timing Logic 2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J6-19	2	Clock (A)	22	W/O
	2	J9-2	2	Clock Ø 2	22	O
	3	J13-3	2	Clock Ø 2	22	BR
	4			8:1 Counter Gate		
	5					
	6	J9-5	2	SOW	22	W/BL
	7	J6-27	2	Sample Pulse (2A)	22	BL
	8	J6-10	2	Sample Pulse Gate (A)	22	BR
	9	J9-7	2	Sample Pulse Gate	22	W/BR
	10	J9-1	2	Data	22	BR
	11	J6-23	2	SOW (A)	22	O
	12	J6-21	2	Data (A)	22	W/G
	13					
	14	J13-4	2	Reset	22	G
	15	J9-3	2	SOW	22	W/Y
	16	J6-30	2	SOW	22	O
	17	J13-2	2	S. R. Gate	22	W/BL
	18	J9-9	2	EOW	22	W/O
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J17

Timing Logic 2A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V(A)-17	1	+12V (A)	20	R
	45	0V(A)-17	1	0V (A)	20	BK
	46	0V(A)-17	1	0V (A)	20	BK
	47	-20V(A)-17	1	-20V (A)	20	S
	48	-20V(A)-17	1	-20V (A)	20	S
	49					
	50	Frame		Chassis Gnd.	20	BK

NOTES:

J18

Timing Logic 2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J6-18	2	Clock (B)	22	W/BR
	2	J10-2	2	Clock Ø 2	22	W/G
	3	J14-3	2	Clock Ø 2	22	Y
③	4	J6-9		8:1 Counter Gate	22	W/O
②	5					
	6	J10-5	2	SOW	22	W/O
	7	J6-29	2	Sample Pulse (2B)	22	G
	8	J6-11	2	Sample Pulse Gate (B)	22	O
	9	J10-7	2	Sample Pulse Gate	22	BL
	10	J10-1	2	Data	22	W/BR
	11	J6-22	2	SOW (B)	22	BR
	12	J6-20	2	Data (B)	22	W/Y
	13					
	14	J14-4	2	Reset	22	W/G
	15	J10-3	2	SOW	22	O
	16	J6-31	2	SOW	22	W/O
	17	J14-2	2	S. R. Gate	22	BL
	18	J10-9	2	EOW	22	G
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J18

Timing Logic 2B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V(B)-18	1	+12V (B)	20	R
	45	0V (B)-18	1	0V (B)	20	BK
	46	0V (B)-18	1	0V (B)	20	BK
	47	-20V(B)-18	1	-20V (B)	20	S
	48	-20V(B)-18	1	-20V (B)	20	S
	49					
	50	Frame		Chassis Gnd	20	BK

NOTES:

J19 POWER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5	AC(Common)-10	1	AC Common	20	W
	6					
	7	F1-2	1	Ac Hot	18	S
	8					
	9	F1-2	1	AC Hot	18	S
	10					
	11					
	12	AC(Hot)-1		AC Switched	18	W/S
	13					
	14	AC(hot)-2		Ac Switched	18	W/S
	15					
	16					
	17					
	18	J1-39	1	-250V (1A)	22	W/V
	19	J2-39	1	-250V (1B)	22	W/V
	20	J3-39	1	-250V (2A)	22	W/V
	21	J4-39	1	-250V (2B)	22	W/V
	22					
	23	J1-38	1	+250V (1A)	22	W/R
	24	J2-38	1	+250V (1B)	22	W/R
	25	J3-38	1	+250V (2A)	22	W/R

NOTES:

J19 POWER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26	J4-38	1	+250V (2B)	22	W/R
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	+12V(A)-19	1	+12V (A Supply)	22	R
	35	-20V(A)-19	1	-20V (A)	22	S
	36	-85V(A)-19	1	-85V (A)	22	W/BK
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V(B)-19	1	+12V (B)	22	R
	45	0V(B)-19	1	0V (B)	22	BK
	46					
	47	-20V(B)-19	1	-20V (B)	22	S
	48					
	49	-85V(B)-19	1	-85V (B)	22	W/BK
	50	Frame		Chassis Gnd	20	BK

NOTES:

J31

POWER SUPPLY A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	AC(Comm)-8	1	AC Common	20	W/S
	2	AC(Comm)-8	1	AC Common	20	W/S
	3					
	4	AC(Hot)-8	1	AC Switched	20	W
	5	AC(Hot)-8	1	AC Switched	20	W
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					

NOTES:

J31

POWER SUPPLY A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	23					
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34			+12V Unregulated		
	35			-20V Unregulated		
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V (A)-1	1	+12V (A)	20	R

NOTES:

J31

POWER SUPPLY A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	45	OV(A)-10	1	OV(A)	20	BK
	46	OV(A)-10	1	OV(A)	20	BK
	47	-20V(A)-1	1	-20V(A)	20	S
	48	-20V(A)-1	1	-20V(A)	20	S
	49	85V(A)-1	1	-85V(A)	20	W/BK
	50	Frame		Chassis Ground	20	BK

NOTES:

J32

POWER SUPPLY B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	AC(Com)-9	1	AC Common	20	W
	2	AC(Com)-9	1	AC Common	20	W
	3					
	4	AC(Hot)-9	1	AC Hot	20	W/S
	5	AC(Hot)-9	1	AC Hot	20	W/S
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					

NOTES:

J32

POWER SUPPLY B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	23					
	24					
	25					
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34			+12V Unreg.		
	35			-20V Unreg.		
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	+12V(B)-1	1	+12V (B)	20	R

NOTES:

J32

POWER SUPPLY B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	45	OV(B)-1	1	OV(B)	20	BK
	46	OV(B)-1	1	OV(B)	20	BK
	47	-20V(B)-1	1	-20V(B)	20	S
	48	-20V(B)-1	1	-20V(B)	20	S
	49	85V(B)-1	1	-85V(B)	20	W/BK
	50	Frame		Chassis Ground	20	BK

NOTES:

+12V(A) BUSS

POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J31-44	1	+12V(A)	20	R
	2					
	3					
	4					
	5	J5-44	1	+12V(A)	20	R
	6	J6A-44	1	+12V(A)	22	R
	7	J7-44	1	+12V(A)	20	R
	8					
	9	J9-44	1	+12V(A)	20	R
	10					
	11	J11-44	1	+12V(A)	20	R
	12					
	13	J13-44	1	+12V(A)	20	R
	14					
	15	J15-44	1	+12V(A)	20	R
	16					
	17	J17-44	1	+12V(A)	20	R
	18					
	19	J19-34	1	+12V (A)	22	R
	20					

NOTES:

OV(A) BUSS

POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-45	1	DLA #1	20	BK
	1	J1-46	1	DLA #1	20	BK
	2					
	3	J3-45	1	DLA #3	20	BK
	3	J3-46	1	DLA #3	20	BK
	4					
	5	J5-45	1	OV(A)	20	BK
	5	J5-46	1	OV(A)	20	BK
	6	J6A-45	1	OV(A)	22	BK
	7	J7-45	1	OV(A)	20	BK
	7	J7-46	1	OV(A)	20	BK
	8					
	9	J9-45	1	OV(A)	20	BK
	9	J9-46	1	OV(A)	20	BK
	10	J31-45	1	OV(A)	20	BK
	10	J31-46	1	OV(A)	20	BK
	11	J11-45	1	OV(A)	20	BK
	11	J11-46	1	OV(A)	20	BK
	12					
	13	J13-45	1	OV(A)	20	BK
	13	J13-46	1	OV(A)	20	BK
	14					
	15	J15-45	1	OV(A)	20	BK
	15	J15-46	1	OV(A)	20	BK
	16					
	17	J17-45	1	OV(A)	20	BK
	17	J17-46	1	OV(A)	20	BK

NOTES:

0V (A) BUSS
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	18					
	19	Frame	Jumper	Chassis Gnd	18	BK
	20	0V(B)-20	Jumper	0V	20	BK

NOTES:

-20V BUSS
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J31-47	1	-20V (A)	20	S
	1	J31-48	1	-20V (A)	20	S
	2					
	2					
	3					
	3					
	4					
	4					
	5	J5-47	1	-20V (A)	20	S
	5	J5-48	1	-20V (A)	20	S
	6	J6A-47	1	-20V (A)	22	S
	7	J7-47	1	-20V (A)	20	S
	7	J7-48	1	-20V (A)	20	S
	8					
	8					
	9	J9-47	1	-20V (A)	20	S
	9	J9-48	1	-20V (A)	20	S
	10					
	10					
	11	J11-47	1	-20V (A)	20	S
	11	J11-48	1	-20V (A)	20	S
	12					
	13	J13-47	1	-20V (A)	20	S
	13	J13-48	1	-20V (A)	20	S
	14					
	15	J15-47	1	-20V (A)	20	S
	15	J15-48	1	-20V (A)	20	S
	16					
	17	J17-47	1	-20V (A)	20	S
	17	J17-48	1	-20V (A)	20	S
	18					

NOTES:

-20V BUSS
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	19	J19-35	1	-20V (A)	22	S
	20					

NOTES:

-85V(A) BUSS
POWER SUPPLY - A

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J31-49	1	-85V(A)	20	W/BK
	2					
	3					
	4					
	5	J5-49	1	-85V(A)	22	W/BK
	6					
	7					
	8					
	9					
	10					
	11	J11-49	1	-85V(A)	22	W/BK
	12					
	13	J13-49	1	-85V(A)	22	W/BK
	14					
	15					
	16					
	17					
	18					
	19	J19-36	1	-85V (A)	22	W/BK
	20					

NOTES:

+12V(B) BUSS

POWER SUPPLY - B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J32-44	1	+12V(B)	20	R
	2					
	3					
	4					
	5	J5A-44	1	+12V(B)	22	R
	6	J6-44	1	+12V(B)	20	R
	7					
	8	J8-44	1	+12V(B)	20	R
	9					
	10	J10-44	1	+12V(B)	20	R
	11					
	12	J12-44	1	+12V(B)	20	R
	13					
	14	J14-44	1	+12V(B)	20	R
	15					
	16	J16-44	1	+12V(B)	20	R
	17					
	18	J18-44	1	+12V(B)	20	R
	19	J19-44	1	+12V (B)	22	R
	20					

NOTES:

OV(B) BUSS

POWER SUPPLY - B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J32-45	1	Power Supply (B)	20	BK
	1	J32-46	1	Power Supply (B)	20	BK
	2	J2-45	1	DLA #2	20	BK
	2	J2-46	1	DLA #2	20	BK
	3					
	4	J4-45	1	DLA #4	20	BK
	4	J4-46	1	DLA #4	20	BK
	5	J5A-45	1	OV(B)	22	BK
	6	J6-45	1	OV(B)	20	BK
	6	J6-46	1	OV(B)	20	BK
	7					
	8	J8-45	1	OV(B)	20	BK
	8	J8-46	1	OV(B)	20	BK
	9					
	10	J10-45	1	OV(B)	20	BK
	10	J10-46	1	OV(B)	20	BK
	11					
	12	J12-45	1	OV(B)	20	BK
	12	J12-46	1	OV(B)	20	BK
	13					
	14	J14-45	1	OV(B)	20	BK
	14	J14-46	1	OV(B)	20	BK
	15					
	16	J16-45	1	OV(B)	20	BK
	16	J16-46	1	OV(B)	20	BK

NOTES:

OV(B) BUSS
POWER SUPPLY - B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	17					
	18	J18-45	1	OV(B)	20	BK
	18	J18-46	1	OV(B)	20	BK
	19	J19-45	1	OV(B)	22	BK
	20	OV(A)-20	Jumper	OV	20	BK

NOTES:

-20V(B) BUSS
POWER SUPPLY - B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J32-47	1	-20V(B)	20	S
	1	J32-48	1	-20V(B)	20	S
	2					
	3					
	4					
	5	J5A-47	1	-20V(B)	22	S
	6	J6-47	1	-20V(B)	20	S
	6	J6-48	1	-20V(B)	20	S
	7					
	8	J8-47	1	-20V(B)	20	S
	8	J8-48	1	-20V(B)	20	S
	9					
	10	J10-47	1	-20V(B)	20	S
	10	J10-48	1	-20V(B)	20	S
	11					
	12	J12-47	1	-20V(B)	20	S
	12	J12-48	1	-20V(B)	20	S
	13					
	14	J14-47	1	-20V(B)	20	S
	14	J14-48	1	-20V(B)	20	S
	15					
	16	J16-47	1	-20V(B)	20	S
	16	J16-48	1	-20V(B)	20	S
	17					
	18	J18-47	1	-20V(B)	20	S
	18	J18-48	1	-20V(B)	20	S

NOTES:

-20V(B) BUSS
POWER SUPPLY - B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	19	J19-47	1	-20V (B)	22	S
	20					

NOTES:

-85V BUSS
POWER SUPPLY - B

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J32-49	1	-85V (B)	20	W/BK
	2					
	3					
	4					
	5					
	6	J6-49	1	-85V (B)	22	W/BK
	7					
	8					
	9					
	10					
	11					
	12	J12-49	1	-85V (B)	22	W/BK
	13					
	14	J14-49	1	-85V (B)	22	W/BK
	15					
	16					
	17					
	18					
	19	J19-49	1	-85V (B)	22	W/BK
	20					

NOTES:

AC SWITCHED BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J19-12	1	AC Switched	18	W/S
	2	J19-14	1	" "	18	W/S
	3	TB1-1	1	" "	18	W/S
	4	J1-34	1	" "	20	W/S
	5	J2-34	1	" "	20	W/S
	6	J3-34	1	" "	20	W/S
	7	J4-34	1	" "	20	W/S
	8	J31-4	1	" "	20	W/S
	8	AC Switched-16 Jumper			20	W/S
	8	J31-5	1	" "	20	W/S
	9	J32-4	1	" "	20	W/S
	9	J32-5	1	" "	20	W/S
	10	J5A-1	1	" "	22	W/S
	11	J6A-1	1	" "	22	W/S
	12					
	13					
	14					
	15					
	16	AC Switched-8 Jumper			20	W/S
	17					
	18					
	19					
	20					

NOTES:

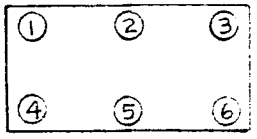
AC COMMON BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F2--2	1	AC Common	18	W
	2	F2--2	1	" "	18	W
	3	TB1-2	1	" "	18	W
	4	J1--36	1	" "	20	W
	5	J2--36	1	" "	20	W
	6	J3--36	1	" "	20	W
	7	J4--36	1	" "	20	W
	8	J31-1	1	" "	20	W
	8	J31-2	1	" "	20	W
	8	AC Com-16	Jumper	" "	20	W
	9	J32-1	1	" "	20	W
	9	J32-2	1	" "	20	W
	10	J19-5	1	" "	20	W
	11	J5A-3	1	" "	22	W
	12	J6A-3	1	" "	22	W
	13					
	14					
	15					
	16	AC Com-8	Jumper		20	W
	17					
	18					
	19					
	20					

NOTES:

SW1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F1-1	1	AC Hot	14	S
	2	J33B	1	AC Hot	14	S
	3					
	4	F2-1	1	AC Common	14	W
	5	J33A	1	AC Common	14	W
	6					



NOTES:

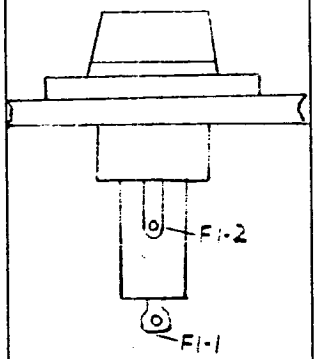
I1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F1-1	1	AC Hot	22	S
	2	F2-1	1	AC Common	22	W

NOTES:

F1

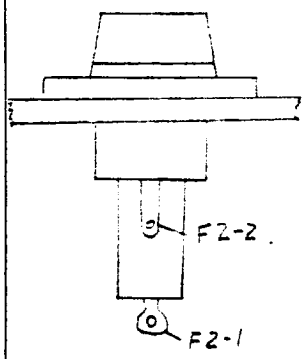
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	SW1-1	1	AC Hot	14	S
	1	I1-1	1	AC Hot	22	S
	2	J19-7	1	AC Hot	18	S
	2	J19-9	1	AC Hot	18	S



NOTES:

F2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	SW1-4	1	AC Common	14	W
	1	I1-2	1	AC Common	22	W
	2	AC(Com)-1	1	AC Common	18	W
	2	AC (Com)-1	1	AC Common	18	W



NOTES:

TB1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	BL1-1	Direct	AC Switched	18	W/S
	1	AC Switched (3)	1	AC Switched	18	W/S
	2	BL1-2	Direct	AC Common	18	W
	2	AC Common (3)	1	AC Common	18	W

NOTES:

BL1 BLOWER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	BL1-1	TB1-1	Direct	AC Switched	18	W/S
	BL1-2	TB1-2	Direct	AC Common	18	W

NOTES:

J42

RECORDER CONNECTOR

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J1-49	2	DLA #1A Output	RG174/U	
	B	J2-49	2	DLA #1B Output	RG174/U	
	C	J3-49	2	DLA #2A Output	RG174/U	
	D	J4-49	2	DLA #2B Output	RG174/U	
	E					
	F					
	G					

NOTES: MS3102A-20-15P

Ground all Coax Shields to the Rack

AC SWITCHED BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J19-12	1	AC Switched	18	W/S
	2	J19-14	1	" "	18	W/S
	3	TB1-1	1	" "	18	W/S
	4	J1-34	1	" "	20	W/S
	5	J2-34	1	" "	20	W/S
	6	J3-34	1	" "	20	W/S
	7	J4-34	1	" "	20	W/S
	8	J31-4	1	" "	20	W/S
	8	AC Switched-16 Jumper			20	W/S
	8	J31-5	1	" "	20	W/S
	9	J32-4	1	" "	20	W/S
	9	J32-5	1	" "	20	W/S
	10	J5A-1	1	" "	22	W/S
	11	J6A-1	1	" "	22	W/S
	12					
	13					
	14					
	15					
	16	AC Switched-8 Jumper			20	W/S
	17					
	18					
	19					
	20					

NOTES:

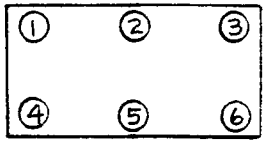
AC COMMON BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F2-2	1	AC Common	18	W
	2	F2-2	1	" "	18	W
	3	TB1-2	1	" "	18	W
	4	J1-36	1	" "	20	W
	5	J2-36	1	" "	20	W
	6	J3-36	1	" "	20	W
	7	J4-36	1	" "	20	W
	8	J31-1	1	" "	20	W
	8	J31-2	1	" "	20	W
	8	AC Com-16	Jumper	" "	20	W
	9	J32-1	1	" "	20	W
	9	J32-2	1	" "	20	W
	10	J19-5	1	" "	20	W
	11	J5A-3	1	" "	22	W
	12	J6A-3	1	" "	22	W
	13					
	14					
	15					
	16	AC Com-8	Jumper		20	W
	17					
	18					
	19					
	20					

NOTES:

SW1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F1-1	1	AC Hot	14	S
	2	J33B	1	AC Hot	14	S
	3					
	4	F2-1	1	AC Common	14	W
	5	J33A	1	AC Common	14	W
	6					



NOTES:

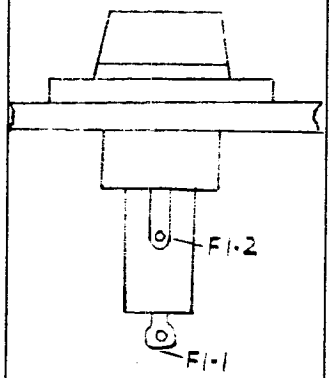
I1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F1-1	1	AC Hot	22	S
	2	F2-1	1	AC Common	22	W

NOTES:

F1

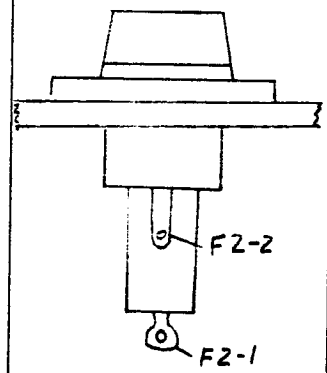
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	SW1-1	1	AC Hot	14	S
	1	I1-1	1	AC Hot	22	S
	2	J19-7	1	AC Hot	18	S
	2	J19-9	1	AC Hot	18	S



NOTES:

F2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	SW1-4	1	AC Common	14	W
	1	I1-2	1	AC Common	22	W
	2	AC(Com)-1	1	AC Common	18	W
	2	AC (Com)-1	1	AC Common	18	W



NOTES:

TB1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	BL1-1	Direct	AC Switched	18	W/S
	1	AC Switched 3	1	AC Switched	18	W/S
	2	BL1-2	Direct	AC Common	18	W
	2	AC Common 3	1	AC Common	18	W

NOTES:

BL1
BLOWER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	BL1-1	TB1-1	Direct	AC Switched	18	W/S
	BL1-2	TB1-2	Direct	AC Common	18	W

NOTES:

CHAPTER IX

SCHEMATICS AND DIAGRAMS

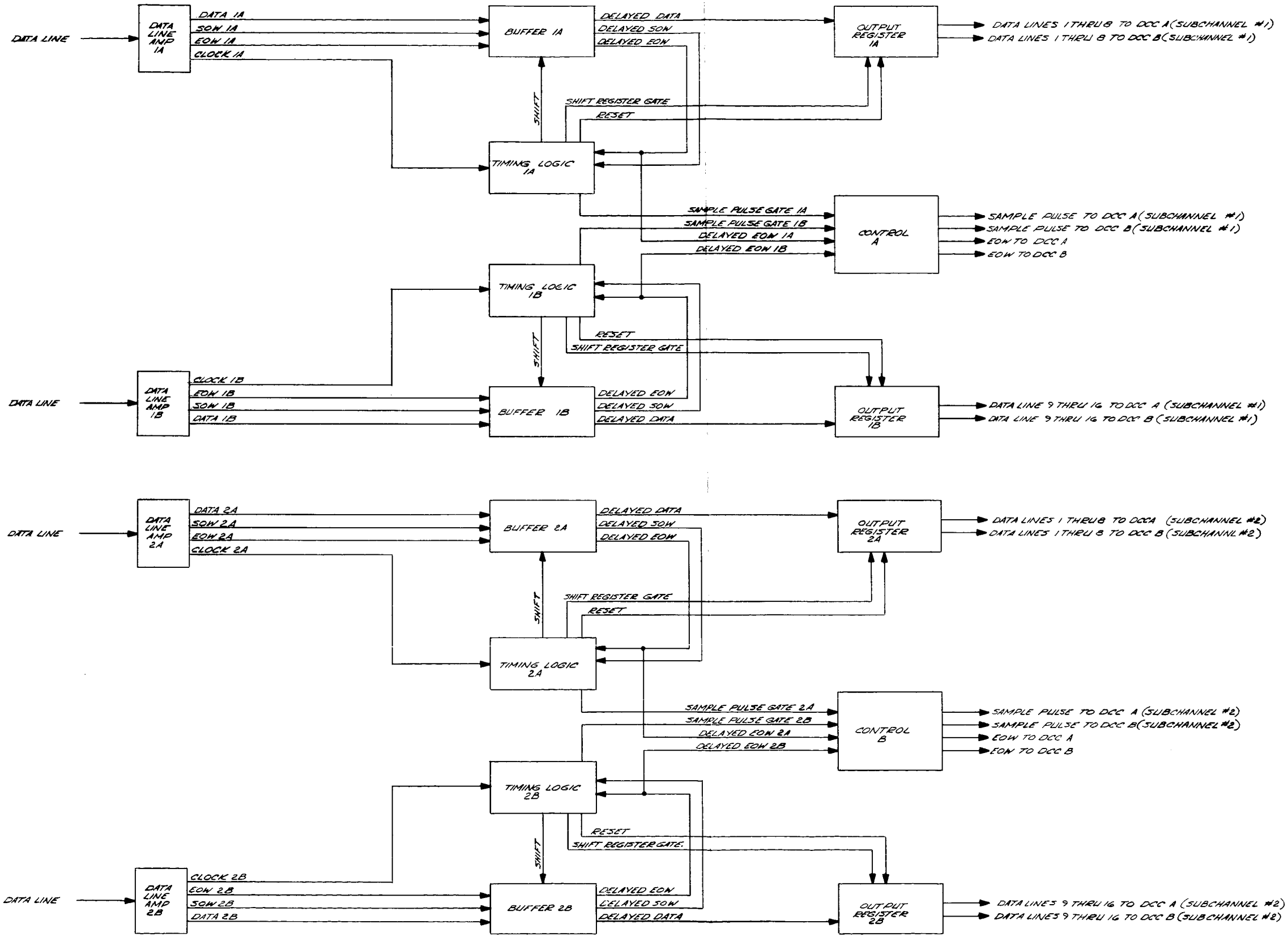


Figure 9-1. Block Diagram,
Model 72 Receiver,
Dwg. #D72B1A
Sheet 1 of 2

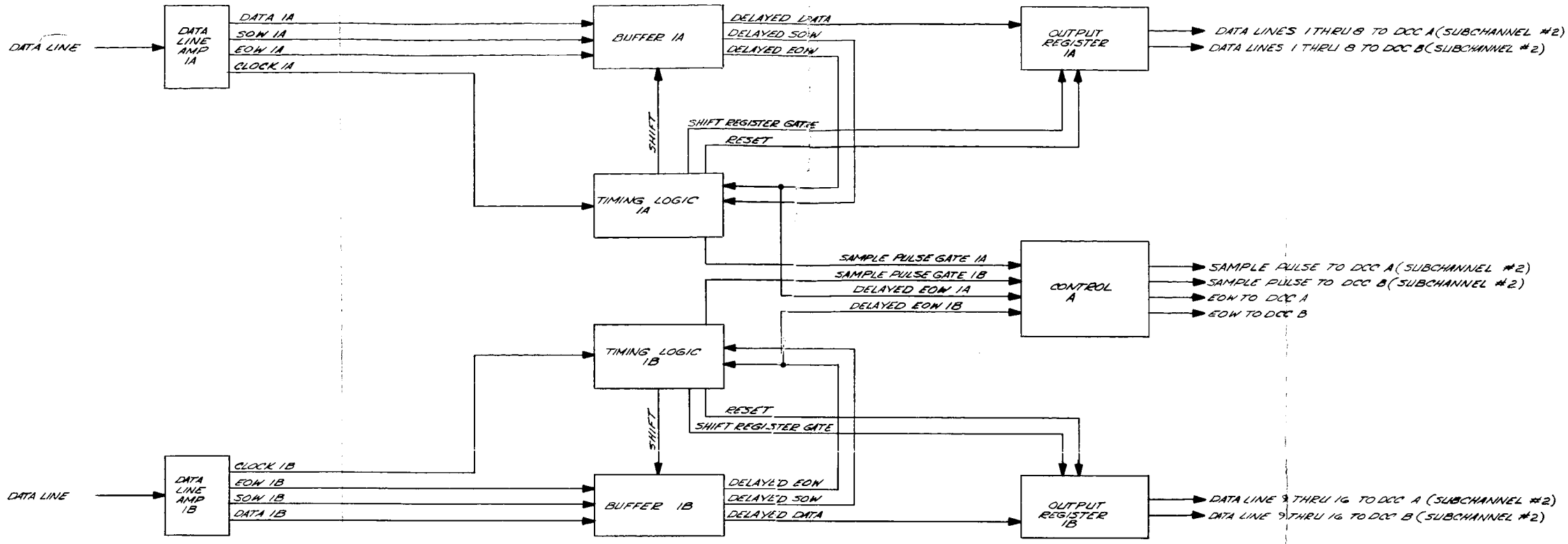


Figure 9-1. Block Diagram, Model 72 Receiver, Dwg. #D72B1A Sheet 1 of 2

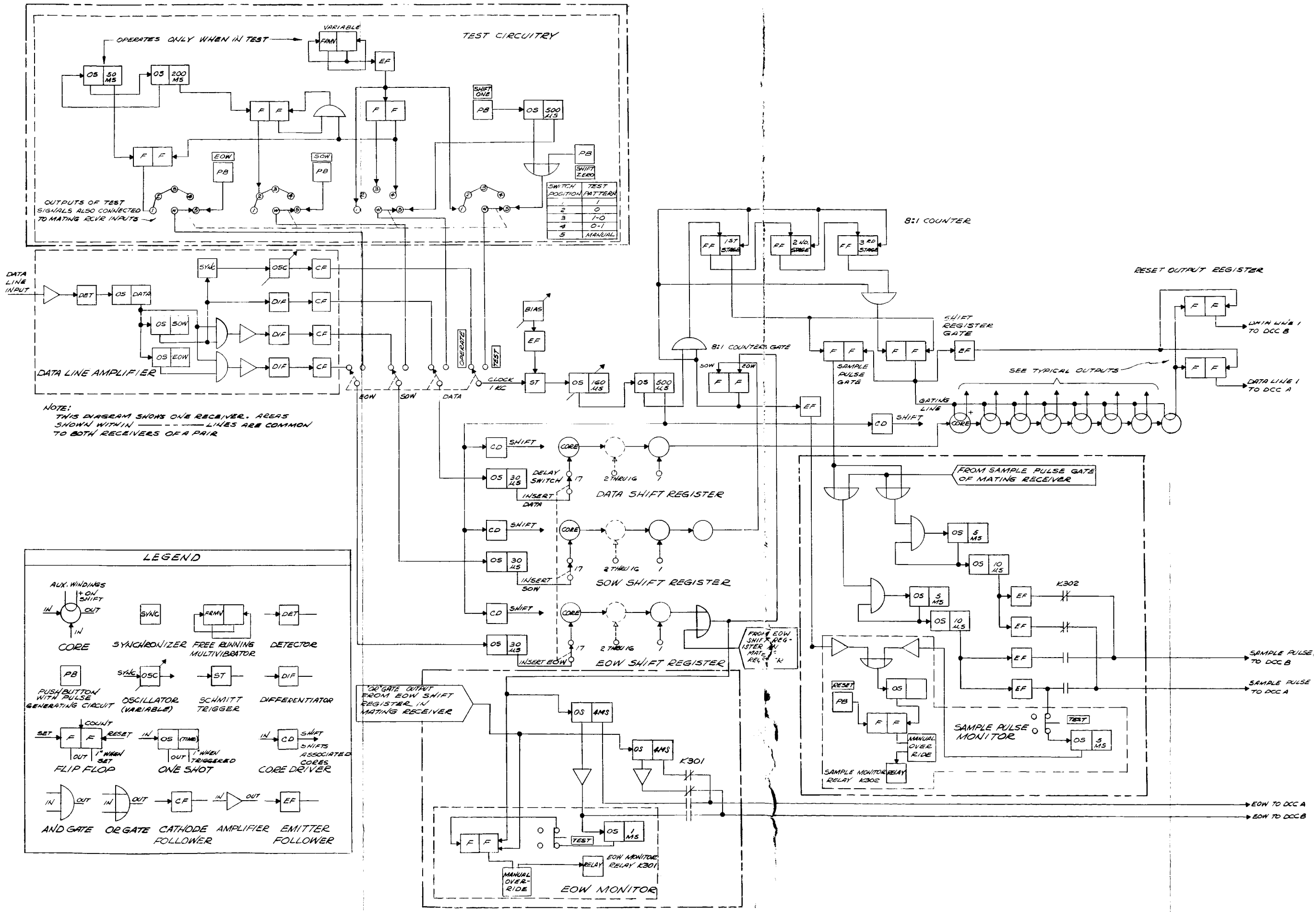
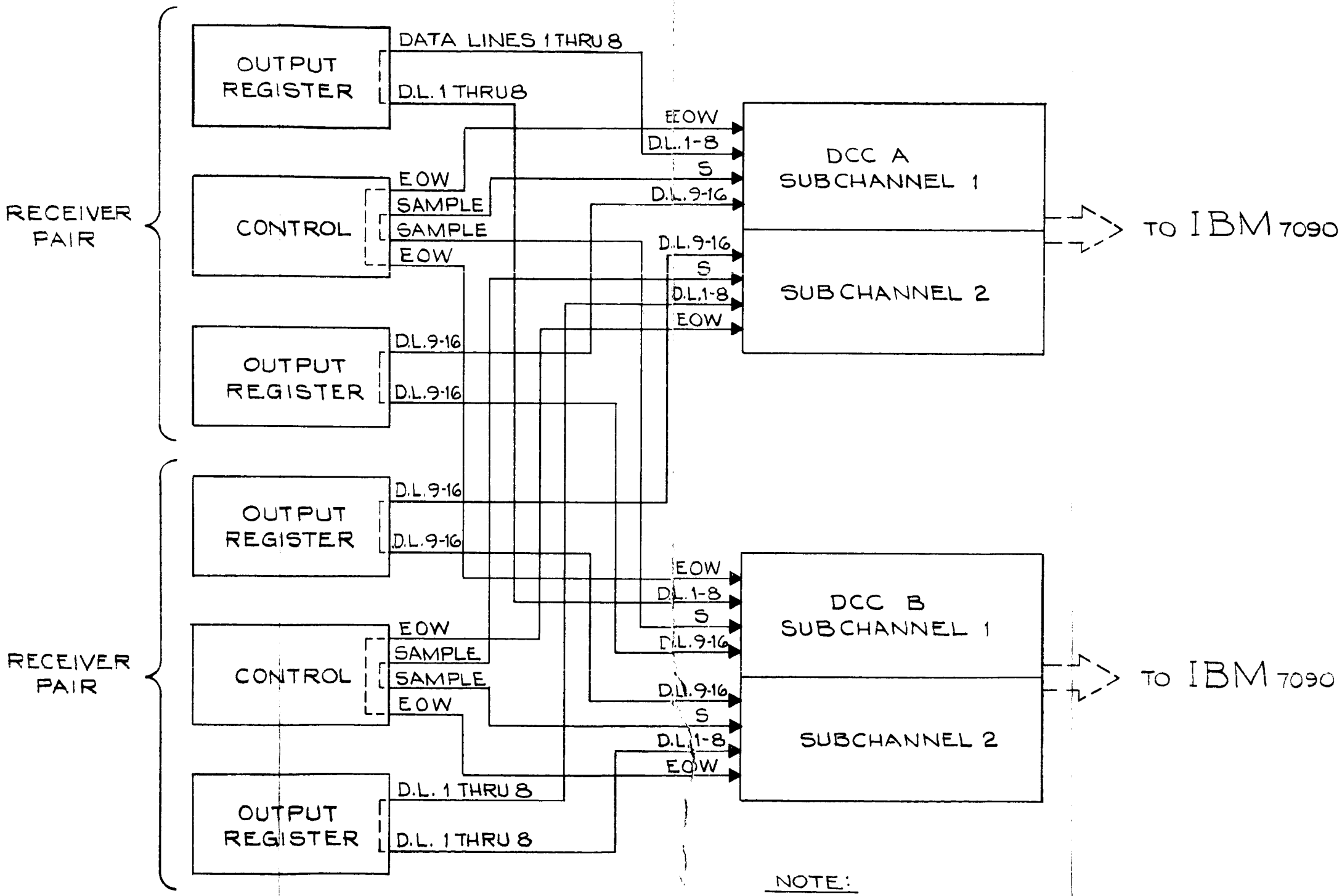


Figure 9-1. Block Diagram, Model 72 Receiver, Dwg. #D72B1A Sheet 2 of 2



NOTE:
GROUND CONNECTIONS NOT SHOWN.

Figure 9-2. Receiver-DCC Connections

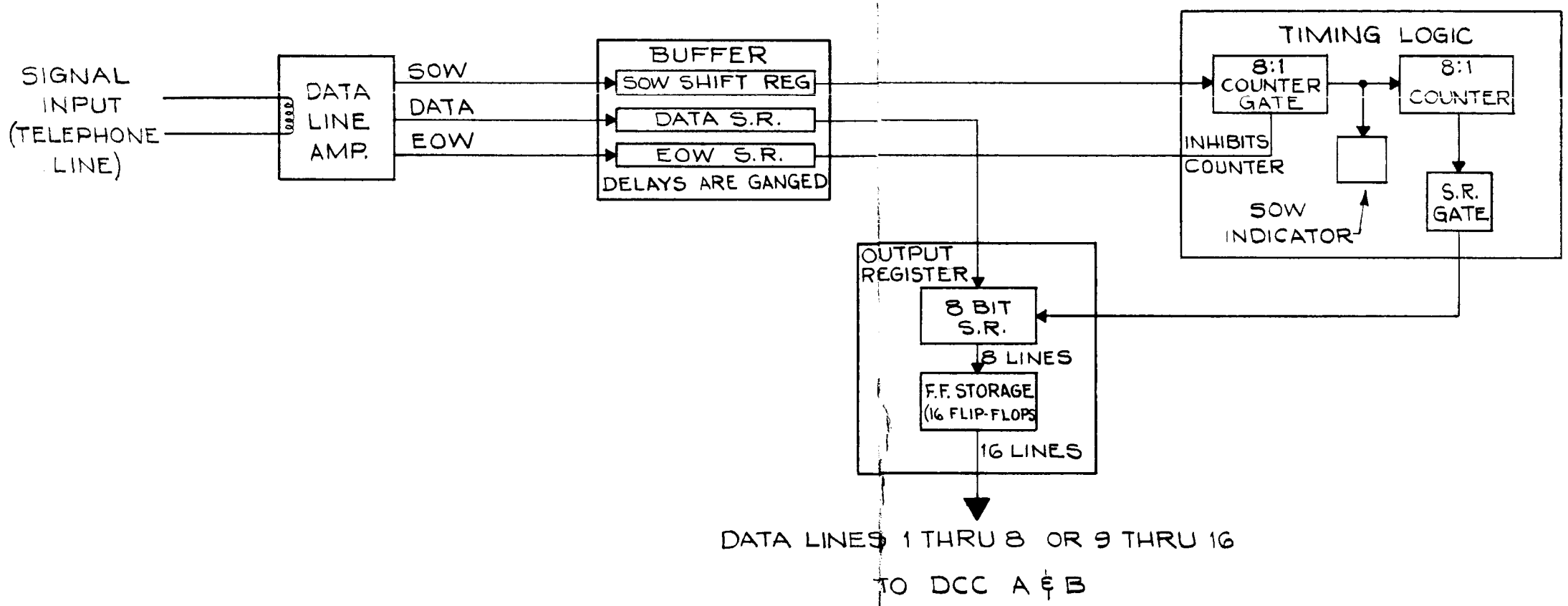


Figure 9-3. Data Flow

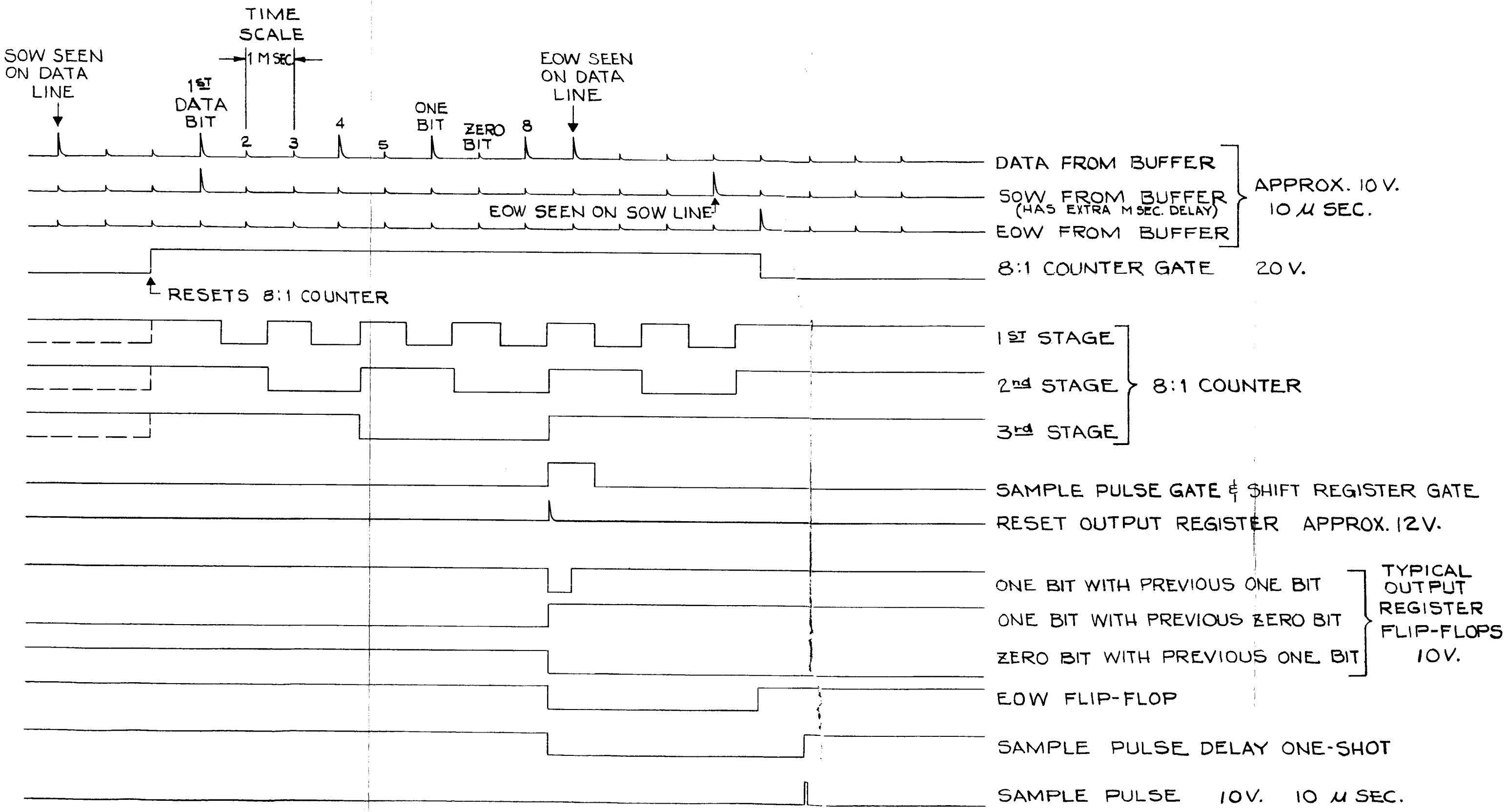
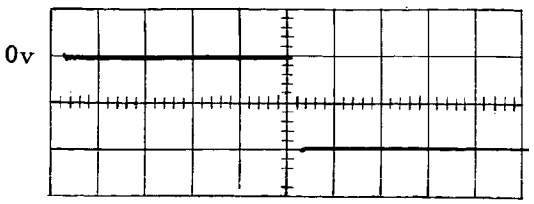
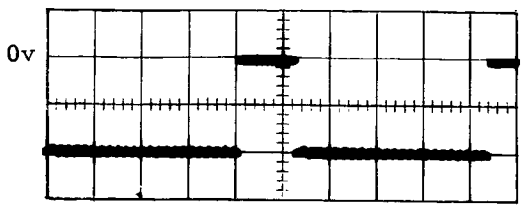
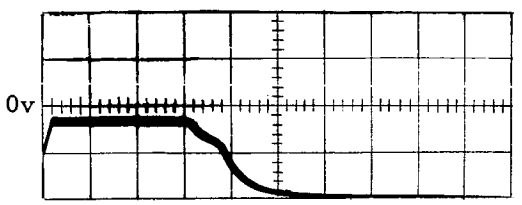
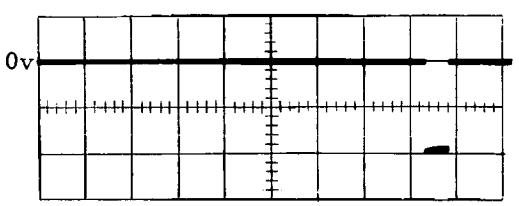
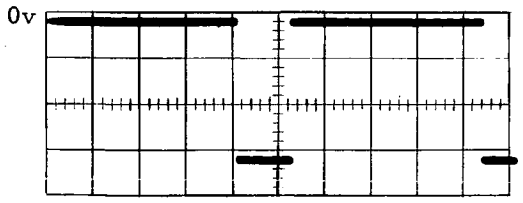
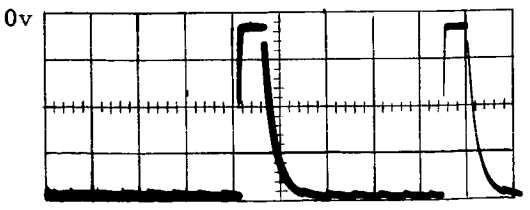
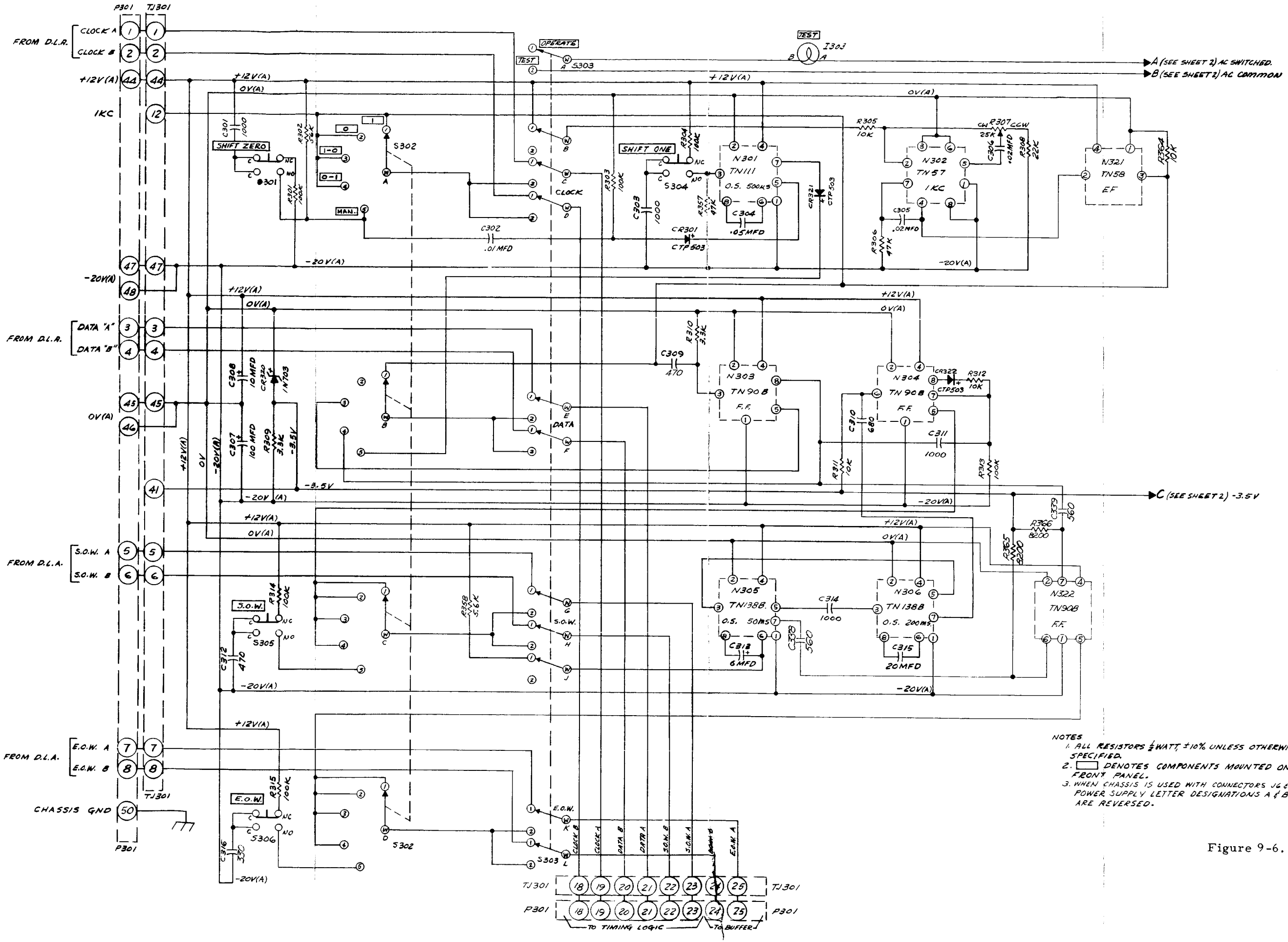


Figure 9-4. Timing Diagram, Dwg. #C72G1A1

	LOCATION	DESCRIPTION
 2 microsec/division and 5v/division	TJ301-28 (72-3A)	Sample Pulse from Control - 10 microsec pulse occurs at 8 MSec intervals indicating data levels are up.
 50 MSec/division and 5v/division	TJ301-33 (72 - 3A)	EOW from Control - 0 volts signifies EOW; level remains until SOW from buffer occurs.
 10 microsec/division and 5v/division	TJ401-4 (72-4A)	Data Bit (one bit) from Buffer - typical core output for a "1".
 1 MSec/division and 5v/division	TJ501-33 (72 - 5A)	Output Data Line from Output Register - a "1" is a 0 volt level, reset occurs at 0.5 MSec before next bit.
 50 MSec/division and 5v/division	TJ601-4 (72 - 6A)	8:1 Counter Gate (timing logic) - 0 volts at SOW from the buffer and 15 volts at EOW from the buffer gates the 8:1 counter ON (at delayed SOW) and OFF (at delayed EOW) and also operates the SOW indicator on the control.
 1 MSec/division and 5v/division	TJ601-17 (72-6A)	Shift Register Gate from the Timing Logic - gates data in the output register from the cores into flip-flops; between 8 and 1 counts of the 8:1 counter. Information is read out of the cores at the midpoint of the positive pulse or at 0.5 MSec after the leading edge of the positive pulse.

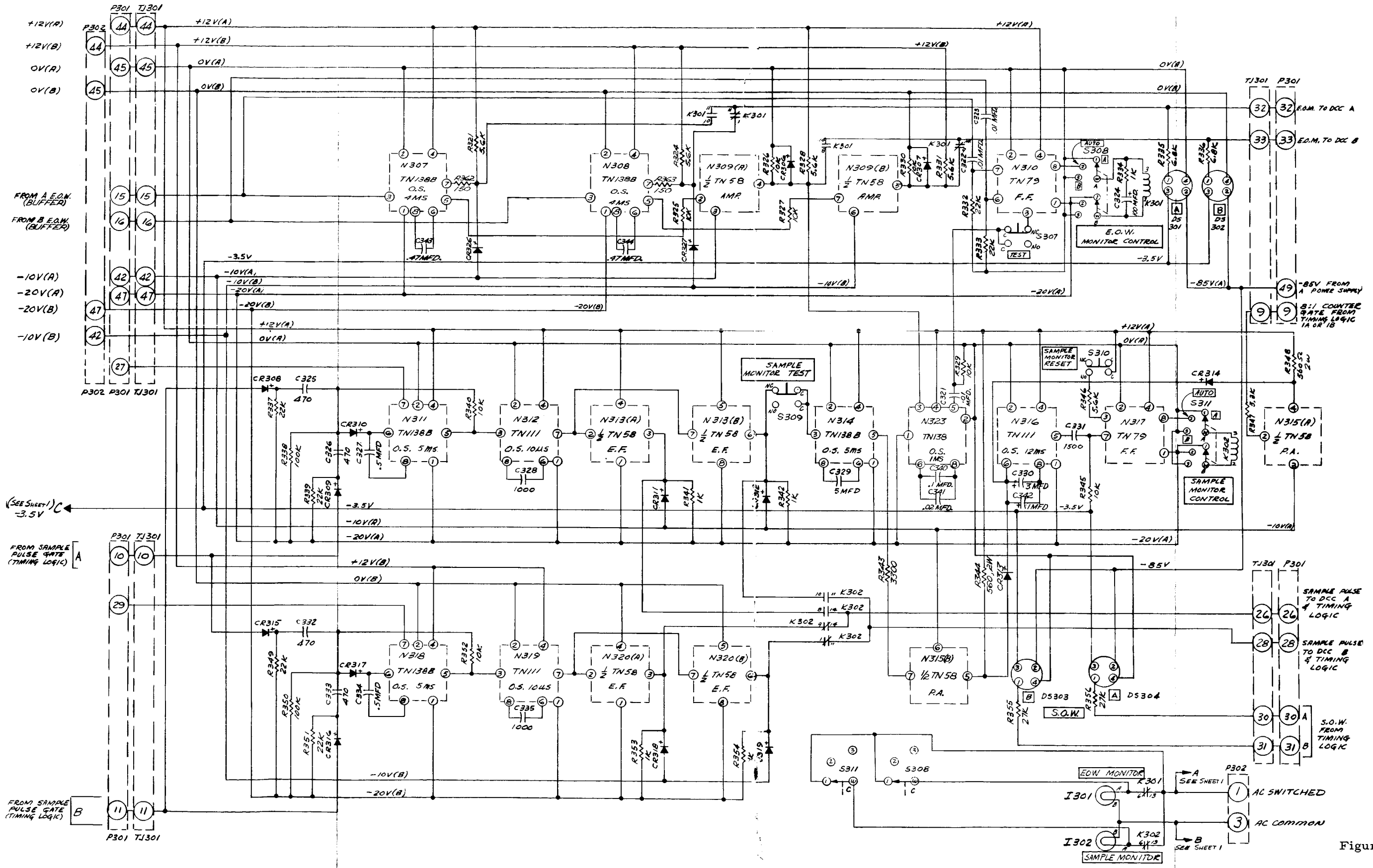
NOTE: These waveforms were taken with the system in test mode with a data pattern of all "1".

Figure 9-5. Waveforms



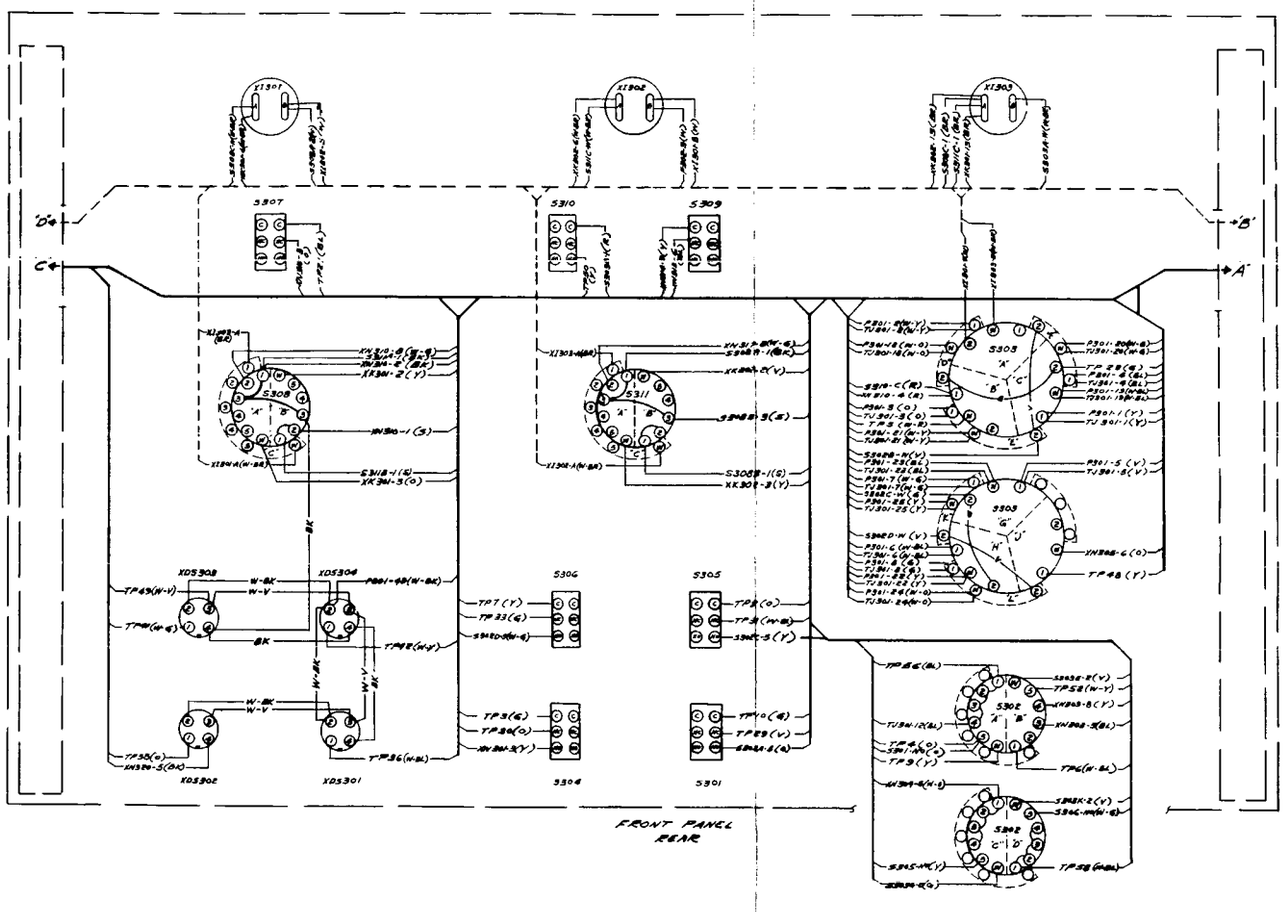
NOTES
1. ALL RESISTORS ¼ WATT ±10% UNLESS OTHERWISE SPECIFIED.
2. ▭ DENOTES COMPONENTS MOUNTED ON FRONT PANEL.
3. WHEN CHASSIS IS USED WITH CONNECTORS J6 & J6A, POWER SUPPLY LETTER DESIGNATIONS A & B ARE REVERSED.

Figure 9-6. Schematic, Control Chassis, Dwg. #D72S3A Sheet 1 of 2



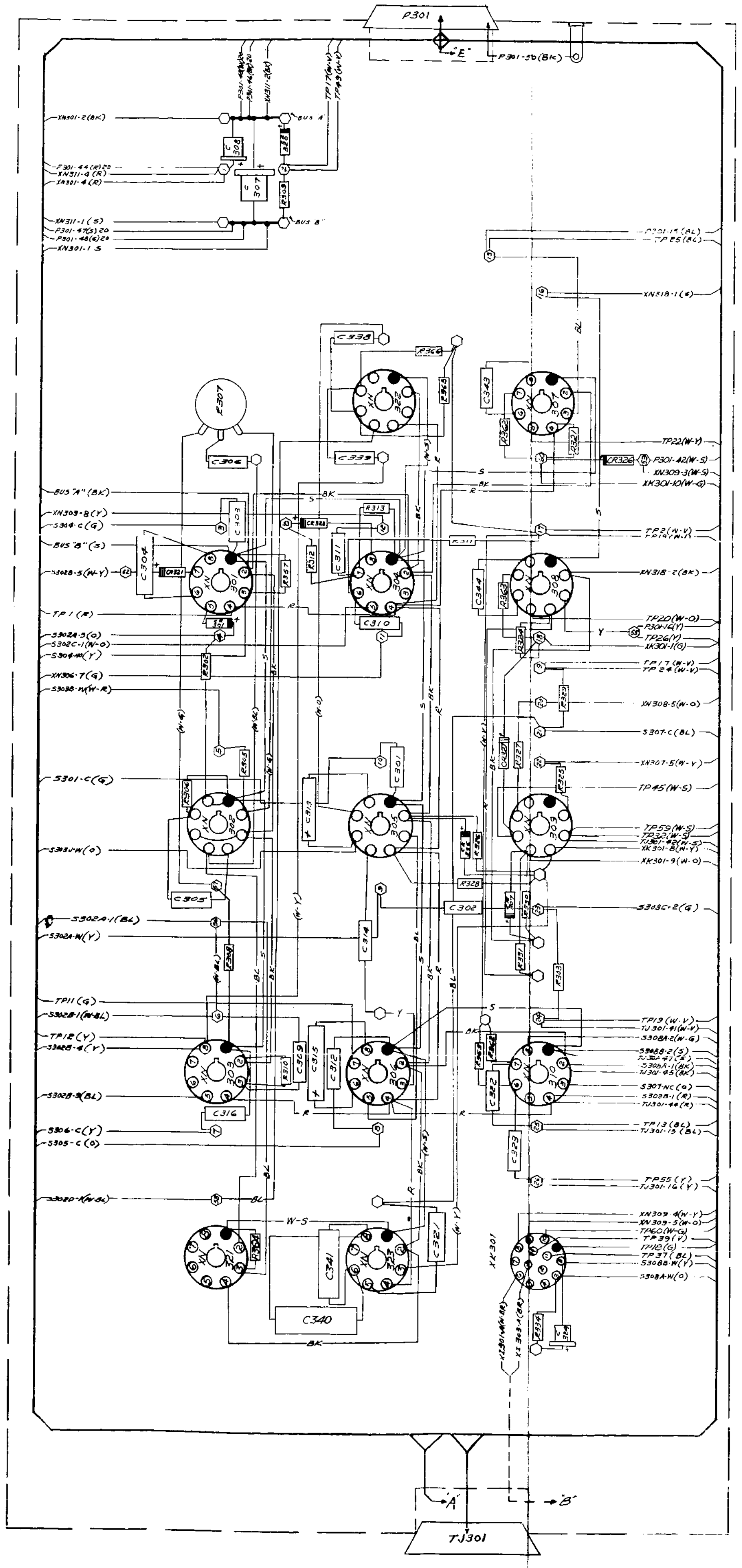
NOTES.
1. ALL RESISTORS ½ WATT ±10% UNLESS OTHERWISE NOTED.
2. ALL DIODES CTP503, OR T12G UNLESS OTHERWISE NOTED.
3. [ ] DENOTES COMPONENTS MOUNTED ON FRONT PANEL.
4. WHEN CHASSIS IS USED WITH CONNECTORS J6 & J8, POWER SUPPLY LETTER DESIG. A & B ARE REVERSED

Figure 9-6. Schematic, Control Chassis, Dwg. #D72S3A Sheet 2 of 2



NOTES:
1. ALL WIRE TO BE #24 UNLESS NOTED.
2. BUS IS DRAWN OUT OF PROPORTION FOR CLARITY.
3. — DENOTES A.C. LEADS / A.C. CABLE.
4. TWIST ALL A.C. LEADS IN PAIRS

Figure 9-7. Wiring Diagram, Control Chassis, Dwg. #E72W3A Sheet 1 of 2



P301

PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	S313C-1	CLOCK A	Y	26	TP 46	SAMPLE TO D.C.C. A	O
2	S303D-1	CLOCK B	(W-Y)	27	XN311-7	SAMPLE TO 8:1 C.G.	O
3	S303E-1	DATA A	O	28	TP 47	SAMPLE TO D.C.C. B	(W-G)
4	S303F-1	DATA B	BL	29	XN318-7	SAMPLE TO 8:1 C.G.	(W-G)
5	S303G-1	S.O.W. A	V	30	TP 43	S.O.W. "A"	Y
6	S303H-1	S.O.W. B	(W-BL)	31	TP 41	S.O.W. "B"	G
7	S303K-1	E.O.W. A	(W-G)	32	TP 37	E.O.W. TO D.C.C. A	BL
8	S303L-1	E.O.W. B	G	33	TP 39	E.O.W. TO D.C.C. "B"	V
9	TP 34	8:1 COUNTER GATE	BL	34			
10	TP 28	FROM SAMPLE PULSE GATE "A"	Y	35			
11	TP 27	FROM SAMPLE PULSE GATE "B"	O	36			
12				37			
13				38			
14				39			
15	TP 13	FROM "A" E.O.W.	BL	40			
16	TP 55	FROM "B" E.O.W.	Y	41			
17				42	XN 319-3	-10 V (A)	(W-S)
18	S303D-W	CLOCK "B"	(W-O)	43			
19	S303C-W	CLOCK "A"	(W-BL)	44	TP 1	+12 V (A)	R(20)
20	S303F-W	DATA "B"	(W-G)	45	BUS "A"	0 V (A)	BK(20)
21	S303E-W	DATA "A"	(W-Y)	46	BUS "A"	0 V (A)	BK(20)
22	S303H-W	S.O.W. "B"	Y	47	BUS "B"	-20 V (A)	S(20)
23	S303G-W	S.O.W. "A"	BL	48	BUS "B"	-20 V (A)	S(20)
24	S303L-W	E.O.W. "B"	O	49	XDS 304-2	-8.5 V (A)	(W-BK)
25	S303K-W	E.O.W. "A"	Y	50	GND. LUG	CHASSIS GND	BK

TJ301

PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	S313C-1	CLOCK A	Y	26	TP 46	SAMPLE TO DCC A	O
2	S303D-1	CLOCK B	(W-Y)	27			
3	S303E-1	DATA A	O	28	TP 47	SAMPLE TO D.C.C. B	(W-G)
4	S303F-1	DATA B	BL	29			
5	S303G-1	S.O.W. A	V	30	TP 43	S.O.W. A	Y
6	S303H-1	S.O.W. B	(W-BL)	31	TP 41	S.O.W. B	G
7	S303K-1	E.O.W. A	(W-G)	32	TP 37	E.O.W. TO DCC "A"	BL
8	S303L-1	E.O.W. B	G	33	TP 39	E.O.W. TO DCC "B"	V
9	TP 34	8:1 COUNTER GATE	BL	34			
10	TP 44	FROM SAMPLE PULSE GATE "A"	Y	35			
11	TP 27	FROM SAMPLE PULSE GATE "B"	O	36			
12	S312A-4	1 KC	BL	37			
13				38			
14				39			
15	TP 25	FROM "A" E.O.W.	BL	40			
16	TP 26	FROM "B" E.O.W.	Y	41	TP 24	-3.5 V	(W-V)
17				42	XN 319-3	-10 V (A)	(W-S)
18	S303D-W	CLOCK B	(W-O)	43			
19	S303C-W	CLOCK A	(W-BL)	44	XN 310-4	+12 V (A)	R
20	S303F-W	DATA B	(W-G)	45	XN 310-2	0 V (A)	BK
21	S303E-W	DATA A	(W-Y)	46			
22	S303H-W	S.O.W. "B"	Y	47	XN 310-1	-20 V (A)	S
23	S303G-W	S.O.W. "A"	BL	48			
24	S303L-W	E.O.W. B	O	49			
25	S303K-W	E.O.W. A	Y	50			

P302

PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XK312-13	A.C. SWITCHED	BR	26			
2				27			
3	XI302-B	A.C. COMMON	W	28			
4				29			
5				30			
6				31			
7				32			
8				33			
9				34			
10				35			
11				36			
12				37			
13				38			
14				39			
15				40			
16				41			
17				42	TP 45	-10 V (B)	(W-S)
18				43			
19				44	XN318-4	+12 V (B)	R
20				45	XN318-2	0 V (B)	BK
21				46			
22				47	XN318-1	-20 V (B)	S
23				48			
24				49			
25				50			

NOTES:
1. ALL WIRE #22 GA UNLESS NOTED
2. --- DENOTES A.C. LEADS & A.C. CABLE
3. TWIST ALL A.C. LEADS IN PAIRS
4. BUS "A" & "B" TO BE #14 BUS

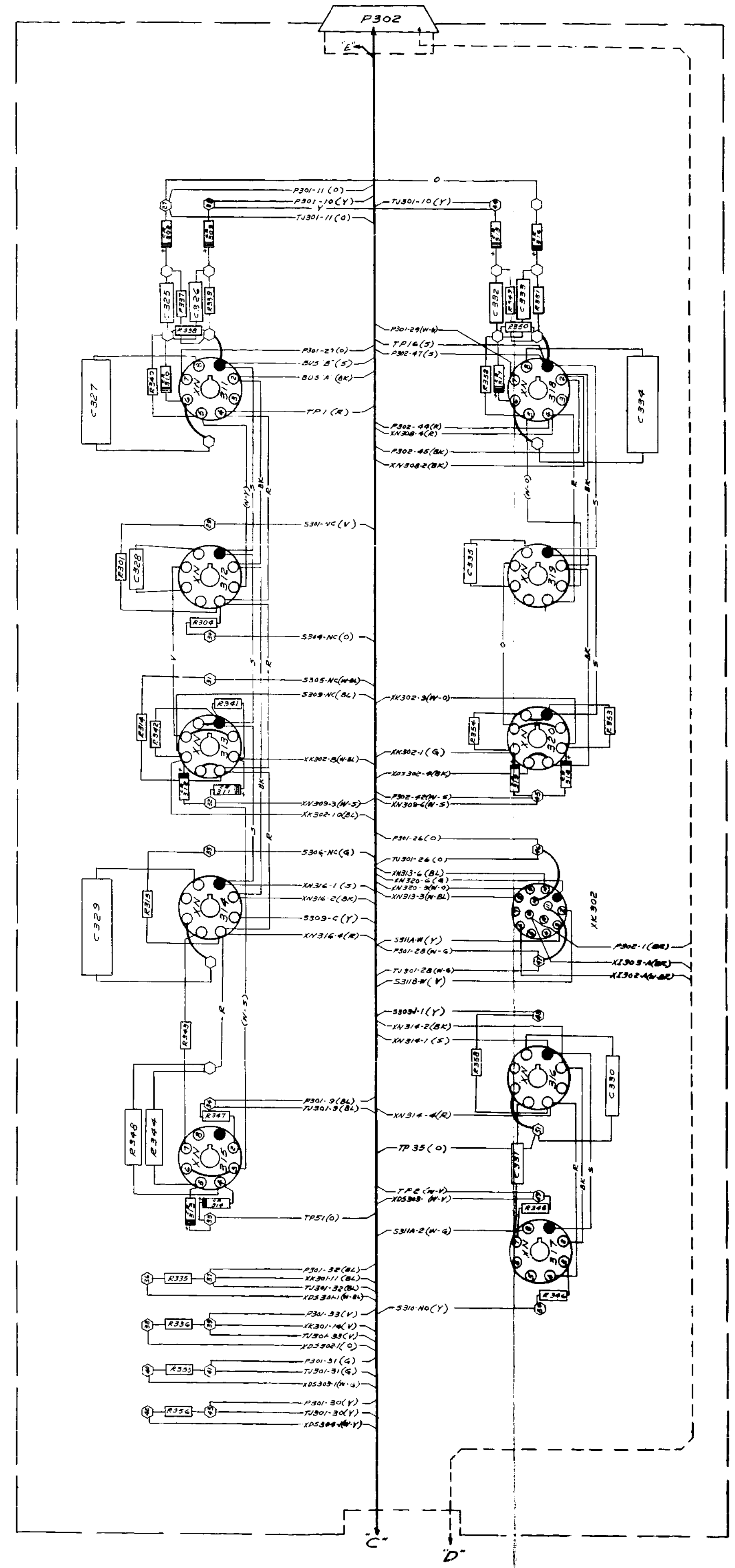
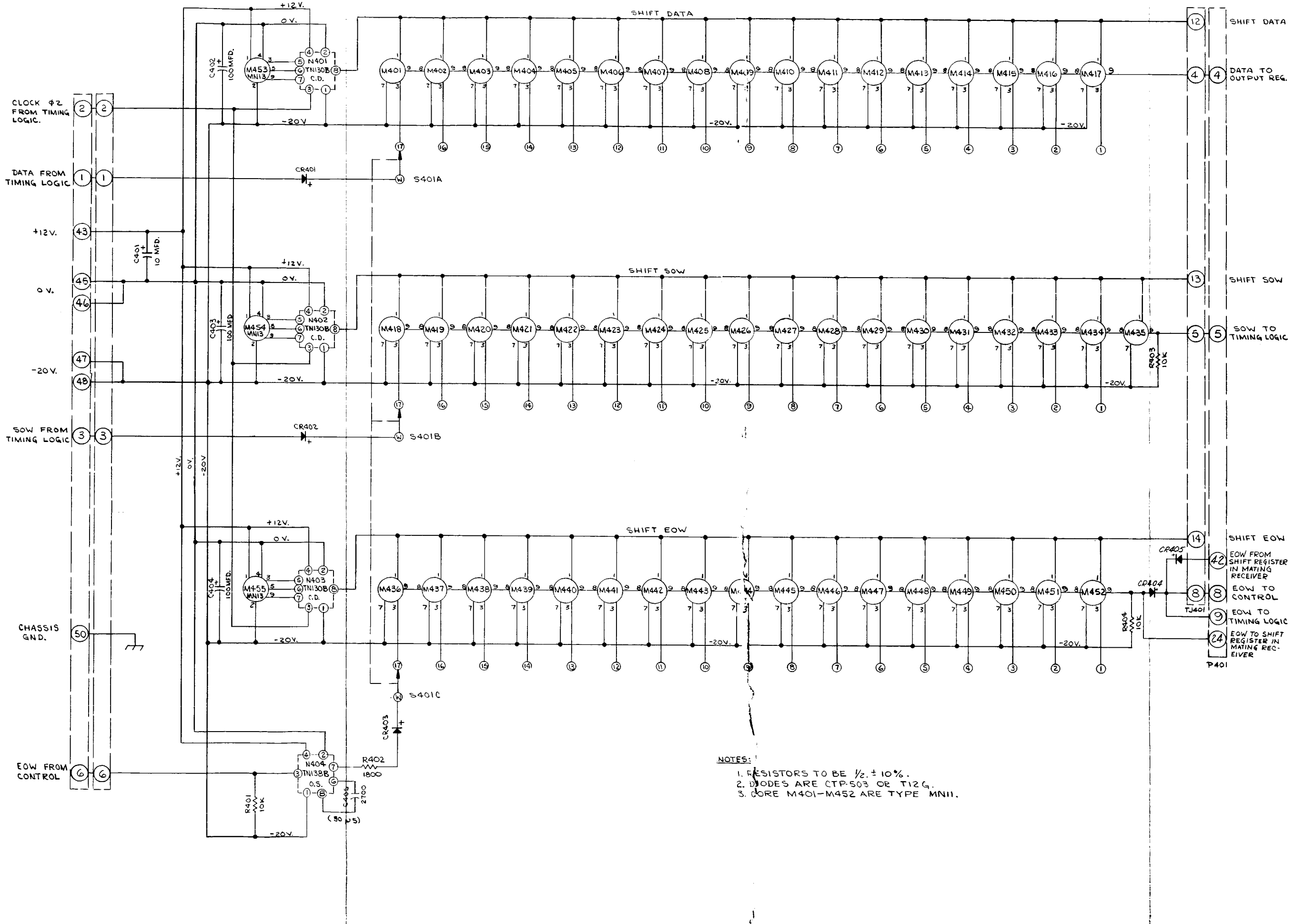


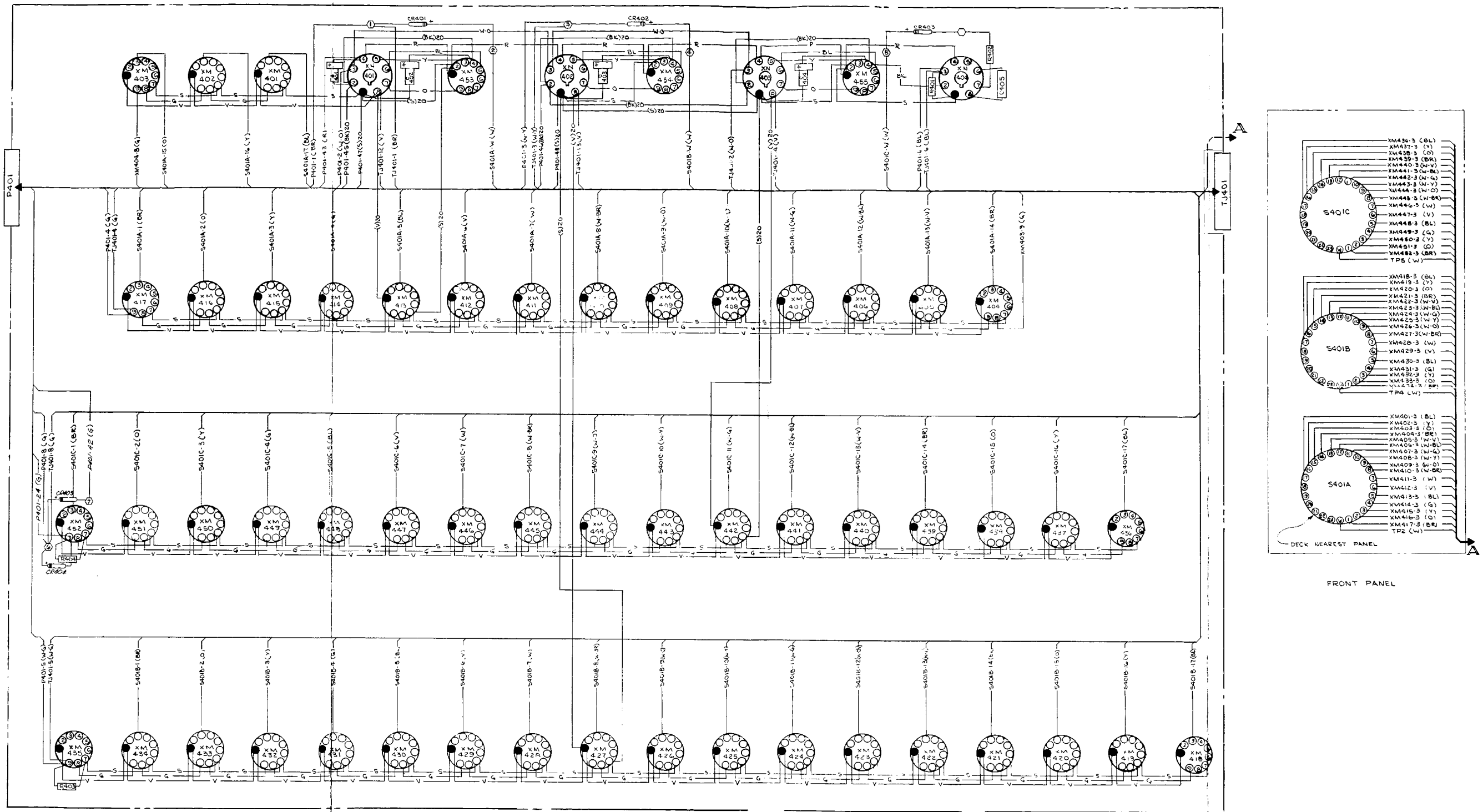
Figure 9-7. Wiring Diagram, Control Chassis, Dwg. #E72W3A Sheet 2 of 2



NOTES:

1. RESISTORS TO BE ½. ± 10%.
2. DIODES ARE CTP-503 OR T12G.
3. CORE M401-M452 ARE TYPE MN11.

Figure 9-8. Schematic, Buffer Chassis, Dwg. #D72S4A



P401

PIN	DESTINATION	FUNCTION	WIRE
1	TP1	DATA FROM TIMING LOGIC	BR
2	XN401-3	CLOCK Ø2	W-O
3	TP3	SOW FROM TIMING LOGIC	W-Y
4	XM417-9	DATA TO SHT. REG.	G
5	XM435-9	SOW TO TIM. LOG.	W-G
6	XN404-3	EOW FROM CONTROL	BL
7			
8	TP-6	EOW TO CONTROL	G
9		EOW TO TIM. LOGIC	
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24	XM432-9	EOW TO FAIRED RCVR	G
25			

PIN	DESTINATION	FUNCTION	WIRE
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42	TP-7	EOW FROM FAIRED RCVR	G
43	XN401-4	+12V.	R
44			
45	XN401-2	0V.	(BK)20
46	XN402-2	0V.	(BK)20
47	XM401-1	-20V	(S)20
48	XM402-1	-20V	(S)20
49			
50	GND. LUG	CHASSIS GND.	BK

TJ401

PIN	DESTINATION	FUNCTION	WIRE
1	TP1	DATA FROM TIMING LOGIC	BR
2	XN403-3	CLOCK Ø2	W-O
3	TP3	SOW FROM TIMING LOGIC	W-Y
4	XM417-9	DATA TO SHT. REG.	G
5	XM435-9	SOW TO TIM. LOG.	W-G
6	XN404-3	EOW FROM CONTROL	BL
7			
8	TP-6	EOW TO CONTROL	G
9			
10			
11			
12	XN401-8	SHIFT DATA	V
13	XN402-8	SHIFT SOW	V
14	XN403-8	SHIFT EOW	V
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			

PIN	DESTINATION	FUNCTION	WIRE
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
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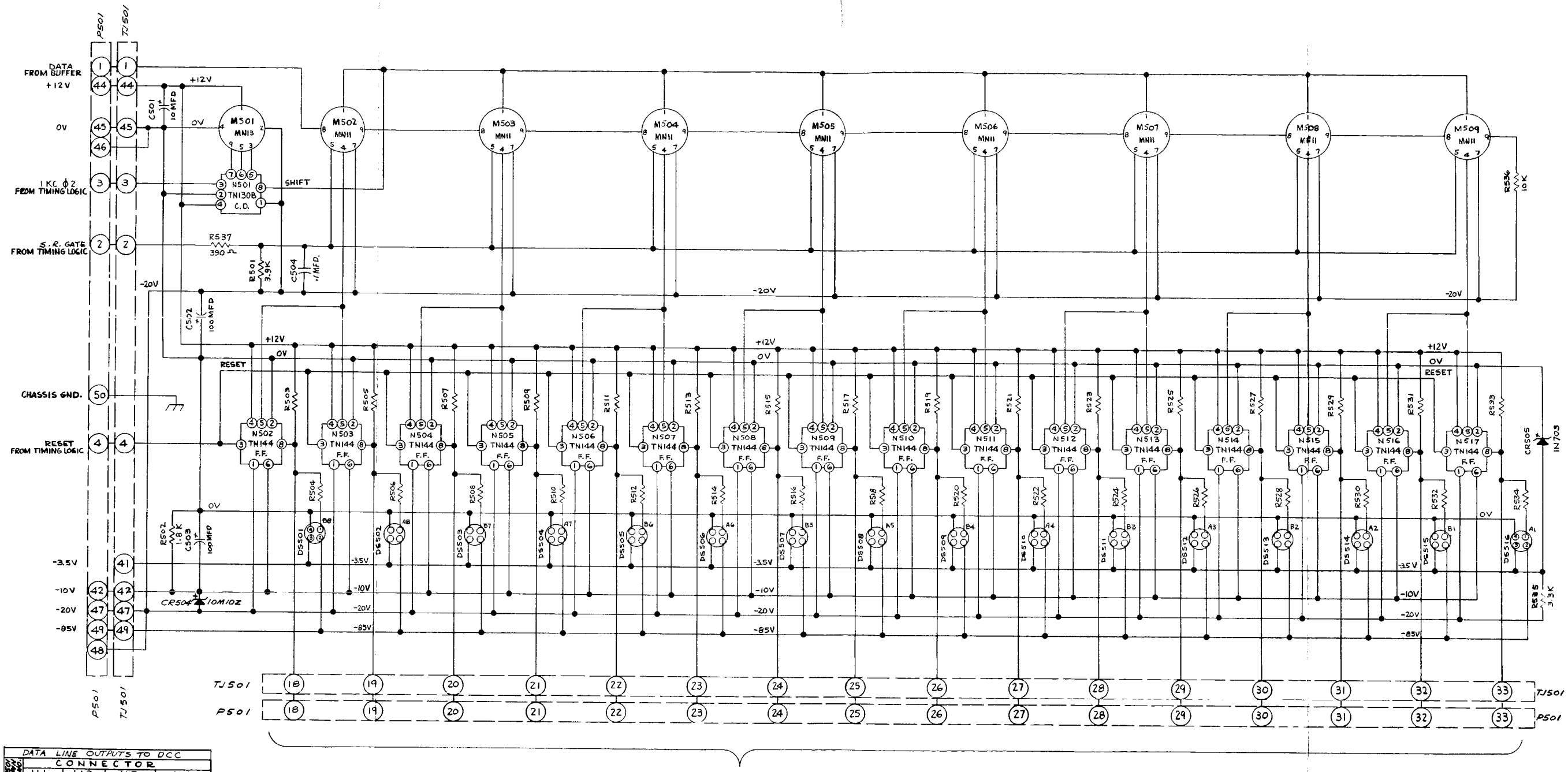
44			
45			
46			
47			
48			
49			
50			

NOTES:
1. ALL WIRES TO BE #22 GA. UNLESS OTHERWISE NOTED.
2. JUMPER PINS 8 & 9 ON P401.

Figure 9-9. Wiring Diagram, Buffer Chassis, Dwg. #E72W4A



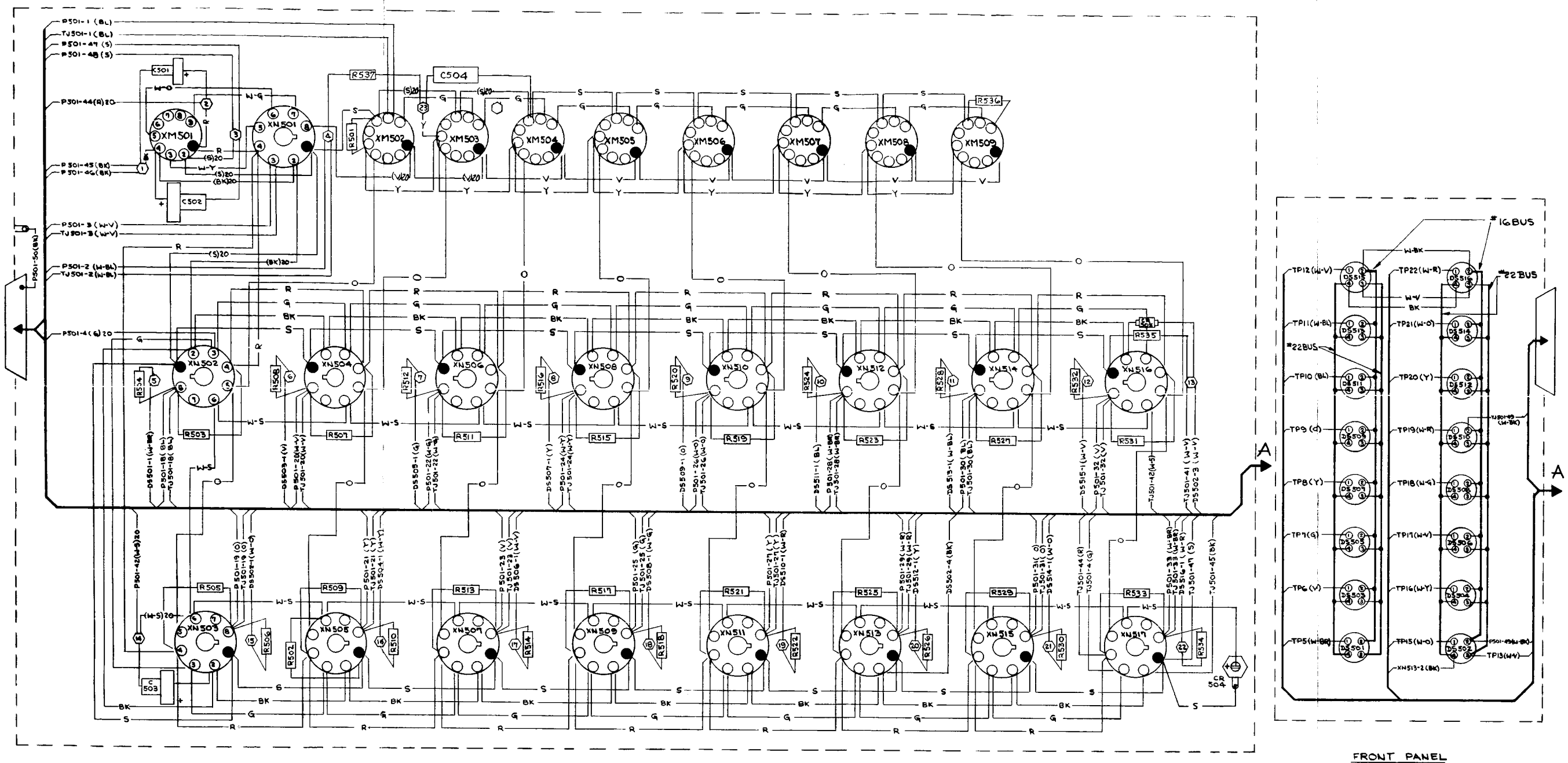
OUTPUTS TO DCC (FORMERLY RTC)

DATA LINE OUTPUTS TO DCC				
	CONNECTOR			
	J11	J12	J13	J14
18	1B8	1B16	2B8	2B16
19	1A8	1A16	2A8	2A16
20	1B7	1B15	2B7	2B15
21	1A7	1A15	2A7	2A15
22	1B6	1B14	2B6	2B14
23	1A6	1A14	2A6	2A14
24	1B5	1B13	2B5	2B13
25	1A5	1A13	2A5	2A13
26	1B4	1B12	2B4	2B12
27	1A4	1A12	2A4	2A12
28	1B3	1B11	2B3	2B11
29	1A3	1A11	2A3	2A11
30	1B2	1B10	2B2	2B10
31	1A2	1A10	2A2	2A10
32	1B1	1B9	2B1	2B9
33	1A1	1A9	2A1	2A9

1ST. DIGIT = SUB CHANNEL
2nd. DIGIT = DCC
3rd. DIGIT = DATA LINE

NOTE:
1. ALL RESISTORS, 5.6K, ½W, ± 10% UNLESS SPECIFIED.

Figure 9-10. Schematic,
Output Register Chassis,
Dwg. #D72S5A

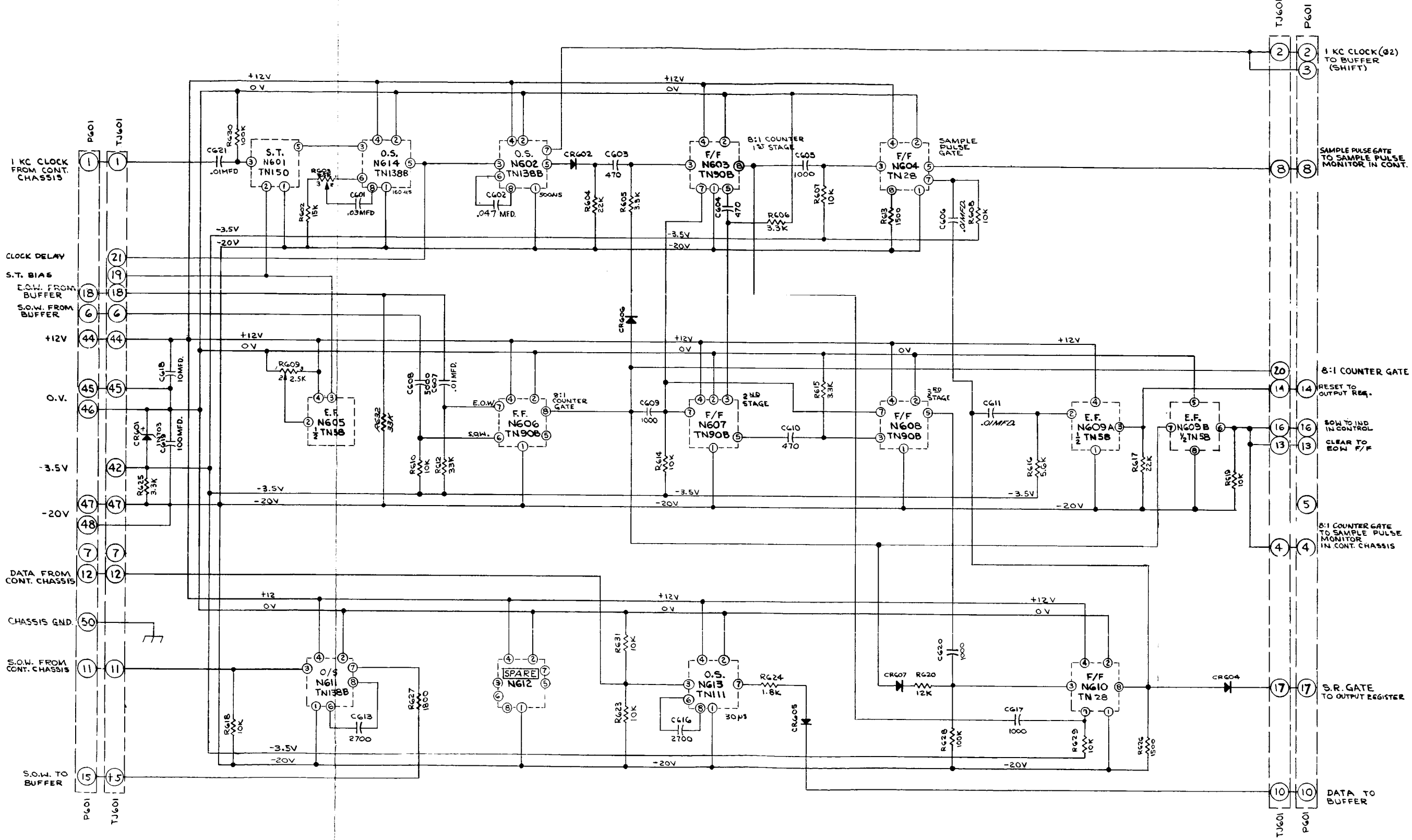


P501							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XM502-B	DATA	BL	26	XN510-B	DATA LINE	W-O
2	TP4	READ OUT GATE	W-BL	27	XN511-B		Y
3	XN501-3	1KC Ø2	W-V	28	XN512-B		W-BR
4	XN502-3	RESET	(G)20	29	XN513-B		W-R
5				30	XN514-B		BL
6				31	XN515-B		O
7				32	XN516-B		V
8				33	XN517-B		W-BR
9				34			
10				35			
11				36			
12				37			
13				38			
14				39			
15				40			
16				41			
17				42	TP16	-10 V.	W-S
18	XN502-B	DATA LINE	BL	43			
19	XN503-B		O	44	TP2	+12V	(R)20
20	XN504-B		W-V	45	TP1	0V	BK
21	XN505-B		Y	46	TP1	0V	BK
22	XN506-B		W-G	47	TP3	-20V	S
23	XN507-B		V	48	TP3	-20V	S
24	XN508-B		W-Y	49	DS502-2	-85V	W-BK
25	XN509-B		G	50	GND LUG	CHASSIS GND	BK

TJ501							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	XM502-B	DATA	BL	26	XN510-B	DATA LINE	W-O
2	TP4	READ OUT GATE	W-BL	27	XN511-B		Y
3	XN501-3	1KC Ø2	W-V	28	XN512-B		W-BR
4	XN517-3	RESET	G	29	XN513-B		W-R
5				30	XN514-B		BL
6				31	XN515-B		O
7				32	XN516-B		V
8				33	XN517-B		W-BR
9				34			
10				35			
11				36			
12				37			
13				38			
14				39			
15				40			
16				41	TP13	-3.5V	W-V
17				42	XN516-6	-10V	W-S
18	XN502-B	DATA LINE	BL	43			
19	XN503-B		O	44	XN517-4	+12V	R
20	XN504-B		W-V	45	XN517-2	0V	BK
21	XN505-B		Y	46			
22	XN506-B		W-G	47	XN517-1	-20V	S
23	XN507-B		V	48			
24	XN508-B		W-Y	49	DS510-2	-85V	W-BK
25	XN509-B		G	50			

NOTES
1-ALL WIRES TO BE #22 GA.
UNLESS OTHERWISE SPECIFY

Figure 9-11. Wiring Diagram, Output Register Chassis, Dwg. #D72W5A



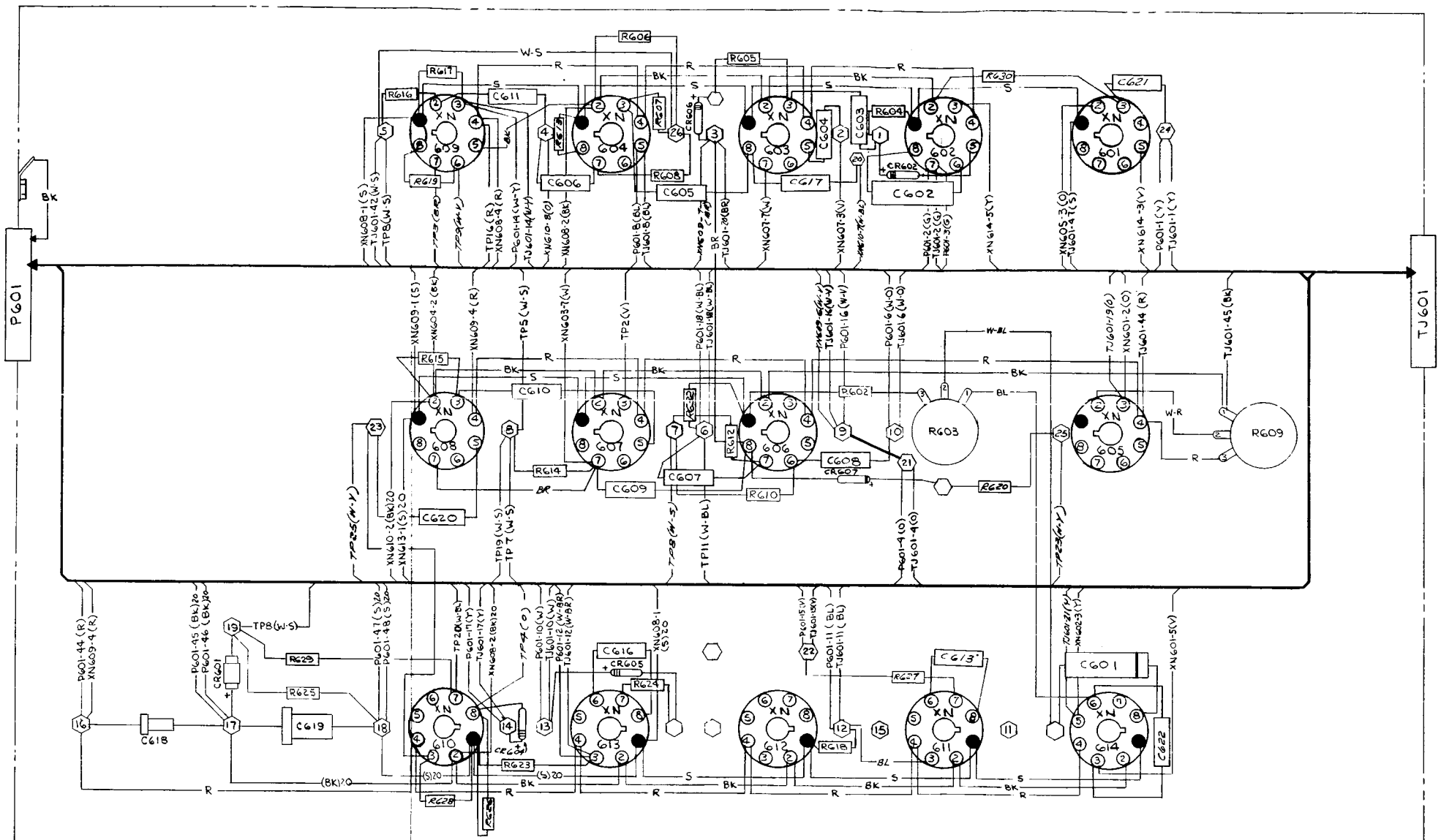
NOTES:

1. ALL RESISTORS TO BE ½ W, ±10% UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES TO BE CTP503 OR T12G UNLESS OTHERWISE SPECIFIED.

Figure 9-12. Schematic,

Timing Logic Chassis,

Dwg. #D72S6A



P601

PIN	DESTINATION	FUNCTION	WIRE
1	XN601-3	IKC	V
2	XN602-7	IKC Ø2	G
3			
4	TP21	8:1 COUNTER GATE	O
5			
6	TP10	SOW	W-O
7			
8	XN604-5	SAMPLE PULSE GATE	BL
9			
10	TP13	DATA	W
11	TP12	SOW	BL
12	XN613-3	DATA	W-BR
13			
14	XN609-3	RESET	W-Y
15	TP22	S.O.W.	V
16	TP9	SOW	W-V
17	TP14	S.R. GATE	Y
18	TP6	EOW	W-BL
19			
20			
21			
22			
23			
24			
25			

PIN	DESTINATION	FUNCTION	WIRE
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44	TP16	+12V	R
45	TP17	0V	BK
46	TP17	0V	BK
47	TP18	-20V	S
48	TP18	-20V	S
49			
50	GND LUG	CHASSIS GND.	BK

TJ601

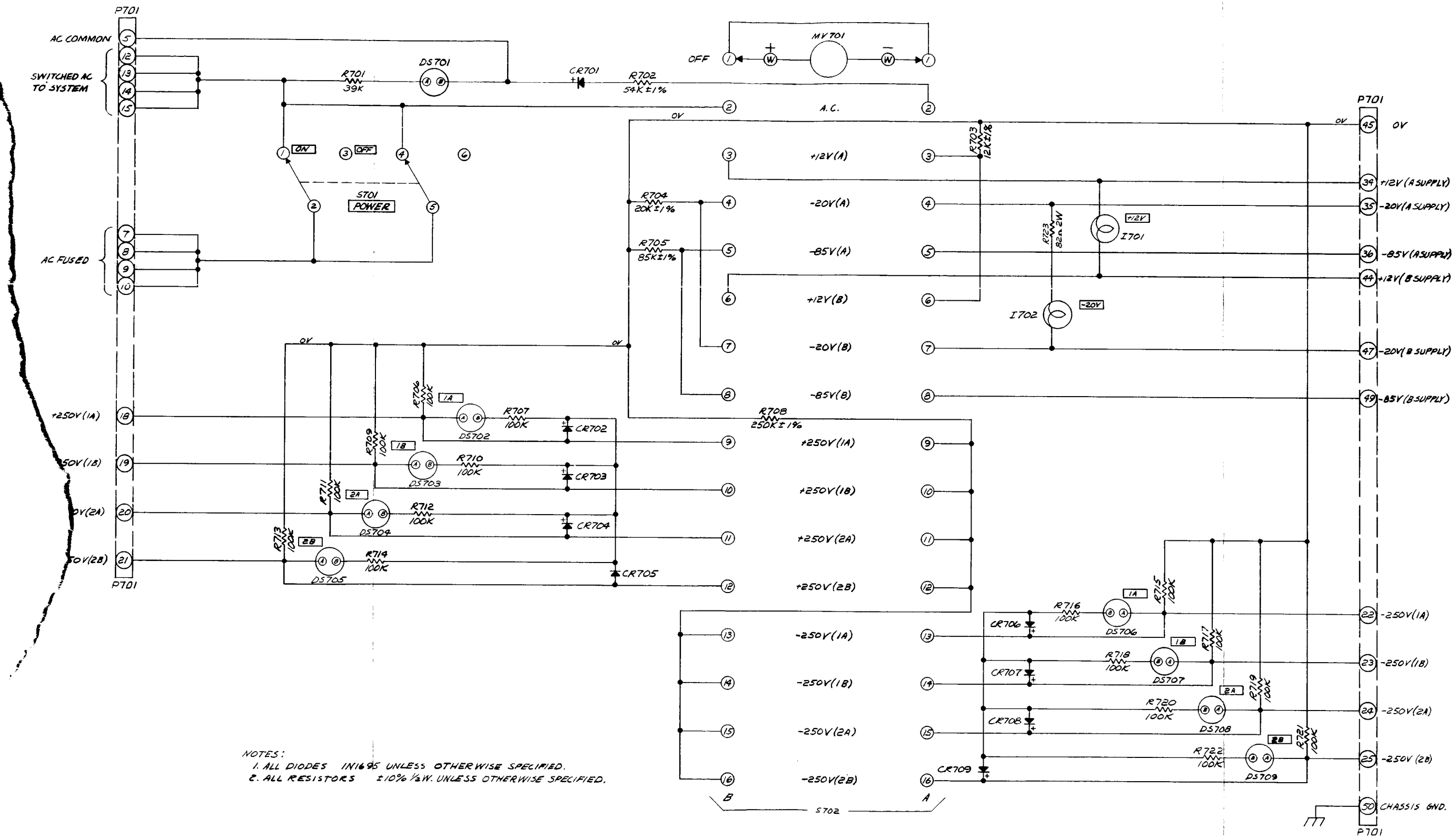
PIN	DESTINATION	FUNCTION	WIRE
1	XN601-3	IKC	V
2	XN602-7	IKC Ø2	G
3			
4	TP21	8:1 COUNTER GATE	O
5			
6	TP10	SOW	W-O
7			
8	XN604-5	SAMPLE PULSE GATE	BL
9			
10	TP13	DATA	W
11	TP12	SOW	BL
12	XN613-3	DATA	W-BR
13			
14	XN609-3	RESET	W-Y
15	TP22	S.O.W.	V
16	TP9	SOW	W-V
17	TP14	S.R. GATE	Y
18	TP6	EOW	W-BL
19	XN605-3	S.T. BIAS	O
20	TP3	8:1 COUNTER GATE	BR
21	XN614-5	CLOCK DELAY	Y
22			
23			
24			
25			

PIN	DESTINATION	FUNCTION	WIRE
26			
27			
28			
29			
30			
31			
32			
33			
34			
35			
36			
37			
38			
39			
40			
41			
42	TP5	-3.5V	W-S
43			
44	XN605-4	+12V	R
45	R609-1	0V	BK
46			
47	XN601-1	-20V	S
48			
49			
50			

NOTE:

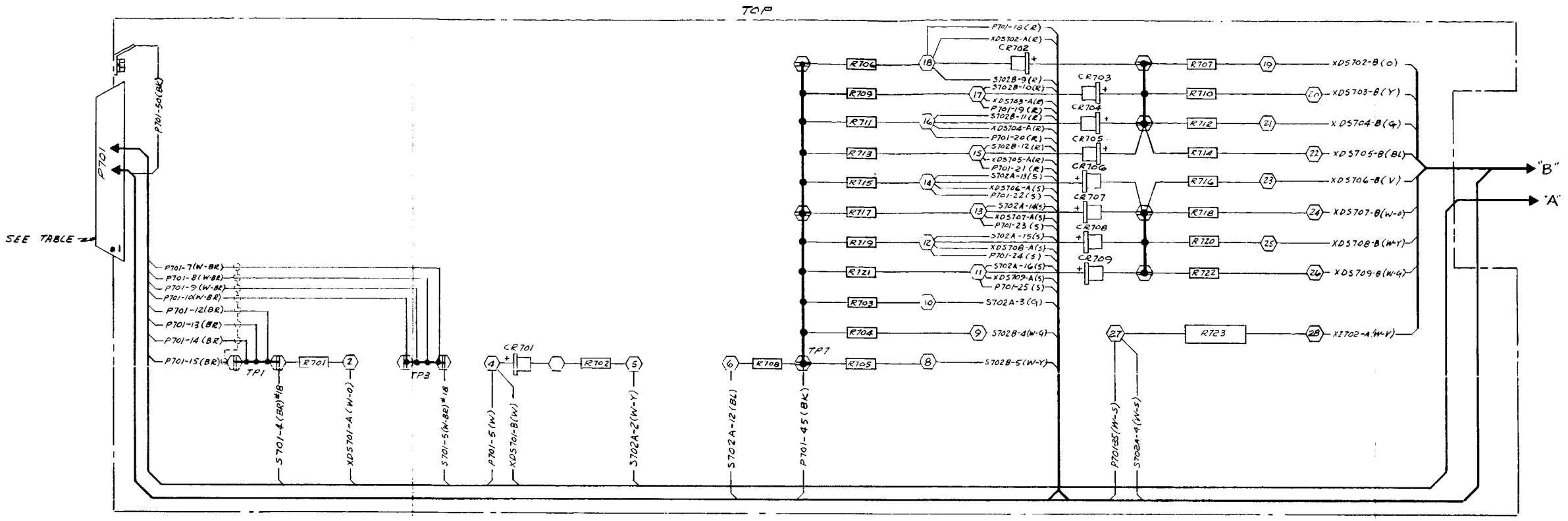
1. ALL WIRE TO BE #22 GA. UNLESS OTHERWISE NOTED.
2. JUMPER TERMINALS ON P601 AS SHOWN IN TABLE.

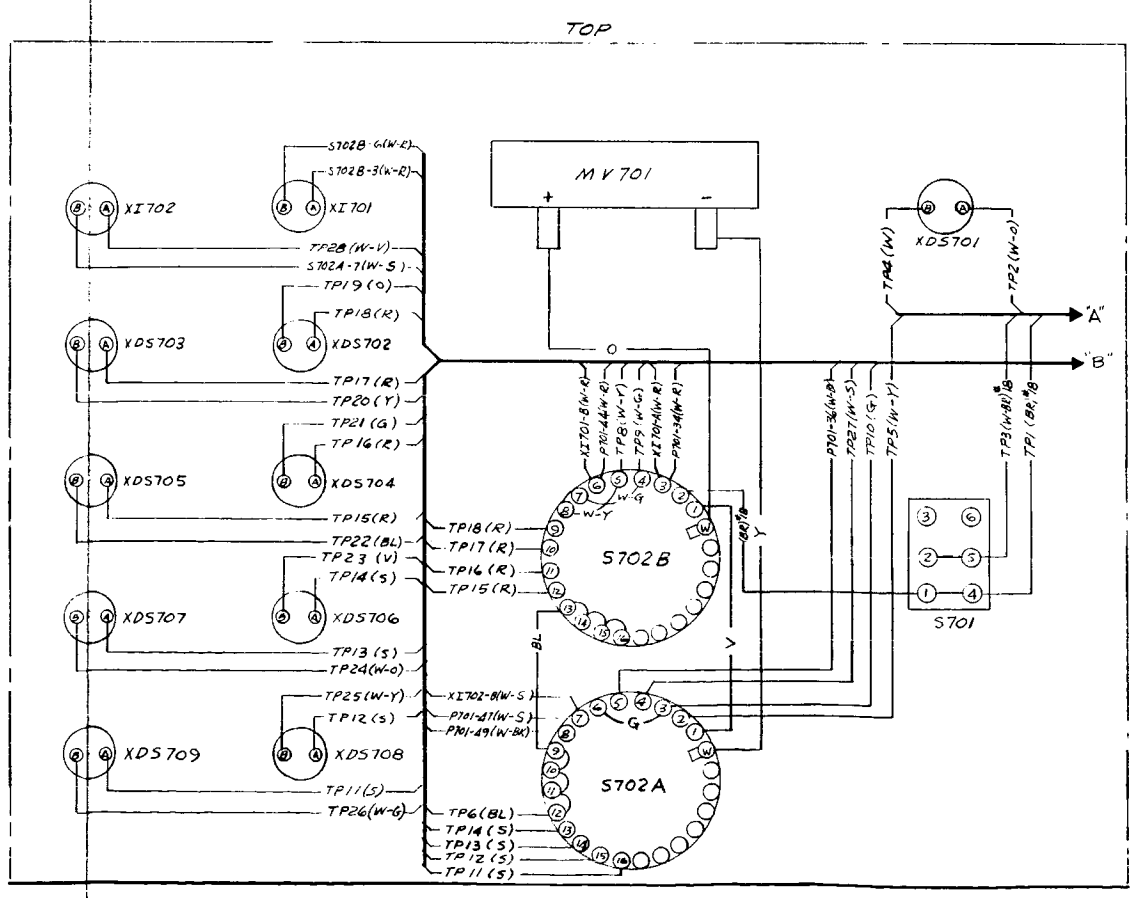
Figure 9-13. Wiring Diagram, Timing Logic Chassis Dwg. #D72W6A



NOTES:
1. ALL DIODES IN1695 UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ±10% ½W. UNLESS OTHERWISE SPECIFIED.

Figure 9-14. Schematic, Power Control Chassis, Dwg. #D72S7A





PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1				26			
2				27			
3				28			
4				29			
5	TP4	AC COMMON	W	30			
6				31			
7	TP3	AC FUSED	W-BR	32			
8	↕	↕	↕	33			
9	↕	↕	↕	34	S702B-3	+12V (A SUPPLY)	W-R
10	TP3	AC FUSED	W-BR	35	TP27	-20V (A SUPPLY)	W-S
11				36	S702A-5	-85V (A SUPPLY)	W-BK
12	TP1	SWITCHED AC TO SYSTEM	BR	37			
13	↕	↕	↕	38			
14	↕	↕	↕	39			
15	TP1	SWITCHED AC TO SYSTEM	BR	40			
16				41			
17				42			
18	TP18	+250V (1A)	R	43			
19	TP17	+250V (1B)	R	44	S702B-6	+12V (B SUPPLY)	W-R
20	TP16	+250V (2A)	R	45	TP7	0V	BK
21	TP15	+250V (2B)	R	46			
22	TP14	-250V (1A)	S	47	S702A-7	-20V (B SUPPLY)	W-S
23	TP13	-250V (1B)	S	48			
24	TP12	-250V (2A)	S	49	S702A-8	-85V (B SUPPLY)	W-BK
25	TP11	-250V (2B)	S	50	GND LUG	CHASSIS GND	BK

NOTES:
1. ⟨ ⟩ DENOTES TWISTED LEADS.
2. S702A DECK NEAREST FRONT PANEL.

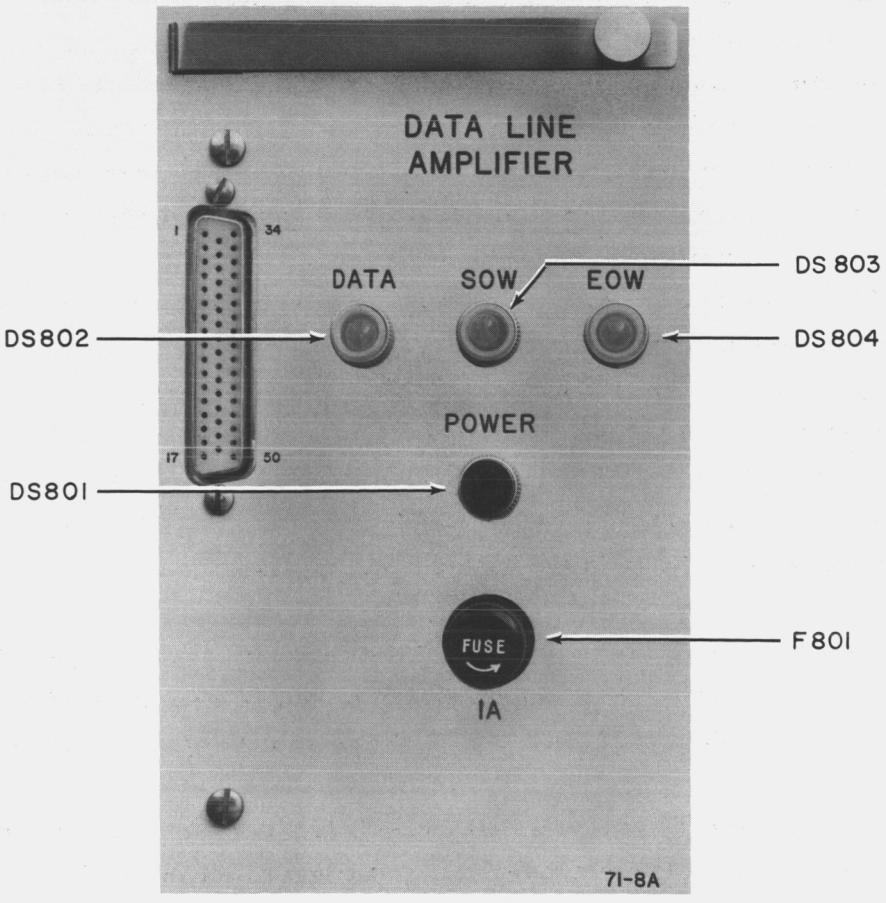
Figure 9-15. Wiring Diagram, Power Control Chassis Dwg. #D72W7A

APPENDIX

DATA LINE AMPLIFIER
MEC MODEL 71-8 A

1. GENERAL

1-1. The Data Line Amplifier receives data in the form of modulated tone bursts of approximately 2 kc at a 1 kc repetition rate from 3 kc voice channels on balanced or unbalanced communication lines, equalized for 1 kc data bit rate. The tone bursts for data are 0.5 milliseconds. The bursts for Start of Word (SOW) and End of Word (EOW) may vary in length depending on the system in which the Data Line Amplifier is used. In some systems, SOW and/or EOW may not be used. The outputs are a 1 kc sinusoidal waveform which is synchronized to data, and pulse outputs of 10 to 20 volts, depending upon termination, approximately 10 microseconds wide, for data, SOW, and EOW. The pulse outputs are cathode follower outputs and require terminating resistors external to the chassis. The Data Line Amplifier Input-Output Relationships figure shows the relationships of incoming and outgoing data. The unit operates on 115 volts ± 10 vac and has a self contained power supply for generating regulated +250 volts and -250 volts for use within the chassis.



Data Line Amplifier

2. DETAILED DESCRIPTION

2-1. Incoming Signals - Data enters the chassis in the form described in paragraph 1-1. at pins 15 and 17 of P801. The inputs are connected to pins 1 and 2 of the bridging transformer T801, which has a 10,000 ohm input impedance. External resistors must be used to match the communication line impedance, normally 600 ohms. This makes it possible for one or more receiving line amplifiers to be used on a single circuit, if so desired. The signal is then filtered in a band pass filter for noise rejection before entering the first stage of amplification. The incoming signal can be seen unfiltered at TJ801, pin 16. However, at this point, the circuit is loaded with the filter impedance and does not give a true representation. The filtered signal can be seen at TJ801, pin 50. Potentiometer R801 provides level selection of the incoming signal to the amplifier and is nominally set for a signal swing of approximately 0.5 volts peak to peak at pin 2 of R801. The filtered signal is a-c coupled to the control grid, pin 1, of V801. This is a remote cut-off pentode tube with AGC applied as bias to the control grid through R802. The signal at the output, pin 5 of V801, is a-c coupled to the grid (pin 2) of V802A which provides the second stage of amplification. The output of V802A pin 1, drives a phase splitter, V802B at pin 7, which has outputs at pins 8 and 6 which are out of phase; that is, when pin 6 is going positive, pin 8 is going negative and vice versa. An output at the junction of R812 and R882 in the cathode of V802B is provided for purposes of recording the data on tape. Each output of the phase splitter drives one-half of V803, a push-pull amplifying stage with a common cathode resistor, R816. The outputs of V803, pins 1 and 6, drive the detector, composed of diodes CR801, CR802, and related circuitry. The anodes of these diodes are clamped to 0 volts by diode CR803. Potentiometer R822 determines the d-c bias at the cathodes of the detecting diodes, and in this way determines the amount of the negative going a-c component of the signal from V803 which will appear at the grid, pin 2 of V804A. V804A is an amplifier which is biased near full conduction by R883 and CR803 which clamps the grid voltage to 0 volts. Negative going pulses from pin 1 or 6 of V803, which exceed the bias voltage determined by R822, cause diode CR801 or CR802 to conduct, turning off V804A and producing a positive pulse at its output, pin 1. Negative pulses at the diode detector output also conduct through diode CR804, are filtered, and applied to the grid of V801, the first stage of the amplifier, for AGC action. The detected signal at the output of V804A is amplified and inverted by V804B which drives the logic circuitry. The waveforms of the detected signal are shown in the Data Line Amplifier Waveform Figure.

2-2. Logic - The negative going edge of the detected signal triggers the data one-shot, V805, a 450 microsecond one-shot, which in turn produces a positive going pulse at pin 6 triggering the SOW one-shot V806, and the EOW one-shot V807; three conditions are now possible:

a. The incoming signal is a data burst. In this case, the data one-shot V805, completes its time delay in 450 microseconds and triggers off the SOW and EOW one-shots as pin 6 of V805 goes negative.

b. The incoming signal is a SOW burst. In this case, the data one-shot continues to receive negative pulses and does not complete its time delay in 450 microseconds. The SOW one-shot V806, is not triggered off, but completes its time delay at a time determined by R849 (normally 2 milliseconds). The EOW one-shot V807, is triggered off by the data one-shot because the incoming code burst has ended (normally 2.5 milliseconds) before the EOW one-shot could complete its time delay.

c. The incoming signal is an EOW burst. When the data one-shot is held on for that duration, both the SOW and EOW one-shots complete their time delays before the data one-shot can trigger them off. The period of the EOW one-shot is determined by R843 and is normally 4 milliseconds.

2-3. As the SOW one-shot is triggered on for every data code burst, its output at pin 6 is used to drive the data output cathode follower at pin 7 of V808. This reduces loading on the data one-shot. The grid of the data cathode follower is biased at approximately -25 volts. The cathode is normally returned through an external resistor to -20 volts. The cathode follower will now conduct when positive pulses occur at the grid, producing a positive output pulse approximately 10 microseconds wide at the mid-point and 20 volts in amplitude, each time there is an incoming data burst, SOW burst, or EOW burst. A neon indicator, DS802, connected to the plate, pin 1, of the data one-shot V805, indicates when data is triggering the data one-shot. This data indicator glows faintly during data absence, but increases in intensity when data is present.

2-4. SOW is recognized by the fact that the SOW one-shot has completed its time delay before the data one-shot has returned to its quiescent state (this will occur for both incoming SOW and EOW). When the incoming signal consists of data bursts, and the SOW one-shot is being triggered on by the leading edge of the data one-shot, and off by the trailing edge, the two one-shot waveforms have basically the same width. The negative going pulse from the data one-shot, pin 1 of V805, is connected to the plate of CR806, which is one leg of a diode gate for detecting SOW. The positive going pulse from the SOW one-shot, pin 6 of V806, is connected to the plate of CR805, which is the remaining leg of the gate for recognizing SOW. When the two pulses to CR805 and CR806 have the same width, the junction of the two diodes is maintained positive, keeping the grid of V810B, pin 7, at a voltage which will retain that half of the tube in full conduction, as diode CR811 clamps the voltage to the grid at 0 volts. Capacitors C817 and C825 filter spikes that occur as a result of slight discrepancies of switching times. When an SOW burst occurs, the SOW one-shot completes its time delay, but the data one-shot is still on. This situation produces a voltage which is approximately +20 volts at the plates of both CR805 and CR806, causing the junction of the two diodes to drop to approximately 20 volts where normally one of the two one-shots had maintained this point at approximately +200 volts. The voltage divider consisting of R834, R835, and R863, which is returned to -250 volts, now produces a negative voltage at the grid (pin 7) of V810

turning the tube off and producing a positive pulse at pin 6, the output. After differentiation, this pulse drives a cathode follower, V808A, which is identical to the data cathode follower just discussed. A neon indicator at the plate, pin 6, of V810B indicates when SOW has been detected. The SOW gate will recognize the same set of circumstances for EOW, as this produces the same condition of the SOW one-shot time delay, ending before the incoming code burst allows the data one-shot to return to its quiescent state.

2-5. EOW is recognized in a similar manner as SOW. The EOW one-shot V807, is triggered on and off by the data one-shot which applies positive and negative pulses at its grid, pin 2. As this one-shot is set for a period exceeding that of the SOW one-shot, when a SOW burst occurs, it will not have completed its time delay before the data one-shot recovers from the SOW burst. On an EOW burst, the same circumstances are produced with the EOW one-shot as just described for the SOW one-shot. The data one-shot produces a negative pulse to the plate of diode CR807, as it did to CR806. The EOW one-shot produces a positive pulse to the plate of diode CR808. During data bursts, the EOW one-shot is triggered off by the data one-shot, and both pulses are of approximately the same width. When an EOW burst occurs, the data one-shot is kept on, and the EOW one-shot completes its time delay. This produces a negative pulse to the grid (pin 2) of V809A similar to that previously discussed for SOW. The output at pin 1 of V809 is a positive pulse for EOW recognition, which drives pin 7 of V809B, the EOW output cathode follower. This cathode follower is identical to the data and SOW cathode followers. A neon indicator is connected to the plate of V809A which indicates the detection of EOW.

2-6. Oscillator - The oscillator within the Data Line Amplifier provides a 1 kc sine wave synchronized to data, and is used by external sources as a means of determining the data bit rate, often referred to as clock. This is necessary as an accurate means of determining whether an absence of data represents one or more 0 bits.

2-6.1. The basic oscillator, V810A, is similar to a standard Colpitts configuration. The frequency is varied by adjusting variable inductor L803. The oscillator is synchronized to incoming data by V811B. Each time a data bit is recognized, one-shot V806 is triggered. Its output, a positive pulse at pin 6, pulses V811B through capacitor C816. Since inductor L803 is in series with the cathode of V811B, each time the tube is pulsed, current flowing through the tube also flows through L803, which is within the tuned circuit of the oscillator. The output of the oscillator, at pin 3, drives a cathode follower, V811A, whose output at pin 3 is a-c coupled to the output terminal, pin 7 of P801, as 1 kc output.

2-7. Power Supply - 115 vac enters the Data Line Amplifier at pins 34 through 37 of P801. DS801 indicates when power is on. The a-c power is connected through fuse F1 to the primary of transformer T802. A secondary, pins 3 and 5, provides 6.3 vac for tube filaments.

A secondary, pins 8 and 10, provides 600 vac center tapped at pin 9 to 0 volts. Three diodes in series are used for rectification to safely meet the voltage requirements. Diodes CR816 through CR821 provide full wave rectification for +250 volts. Resistors R873, R878, and R879 and capacitors C834A and C834B provide filtering. Regulation of the +250 volts is performed by two VR tubes in series, V814 and V815. Half wave rectification, via diodes CR822 through CR824, is used for -250 volts. Filtering and regulation are similar to the +250 volt supply.

2-8. Adjustment - Three basic types of adjustments are to be made on the Data Line Amplifier.

2-8.1. Oscillator - The oscillator frequency is adjusted to 1 kc by adjusting variable inductor L803. Before the oscillator can be properly adjusted, the synchronizing effect of incoming data must be removed. One method of accomplishing this is to adjust R801 until the center tap is at 0 volts. The oscillator no longer receives sync pulses and is then in a free-running condition. Using a dual-trace oscilloscope such as a Tektronix 545A with CA plug-in, synchronize and put one trace on a good 1 kc source. If a local source is not available, data from a Data Line Amplifier, preferably with an input test pattern of all "1"s offers a suitable source. Use the remaining trace to observe pin 3 of tube V810. L803 should be adjusted to produce a frequency equal to the test frequency. By ultimately using a sweep on the scope which displays only one or two cycles, the operator can insure that the two signals are actually at the same frequency.

NOTE

At relatively slow sweeps, the two waveforms may have the appearance of being synchronized. If going to a faster sweep results in double traces, the two waveforms are not yet synchronized.

Rolling of one trace with respect to the other should be expected, but it is readily possible to adjust the oscillator to within a few cycles per second of the external source. A normal adjustment of ±3 cps is satisfactory.

NOTE

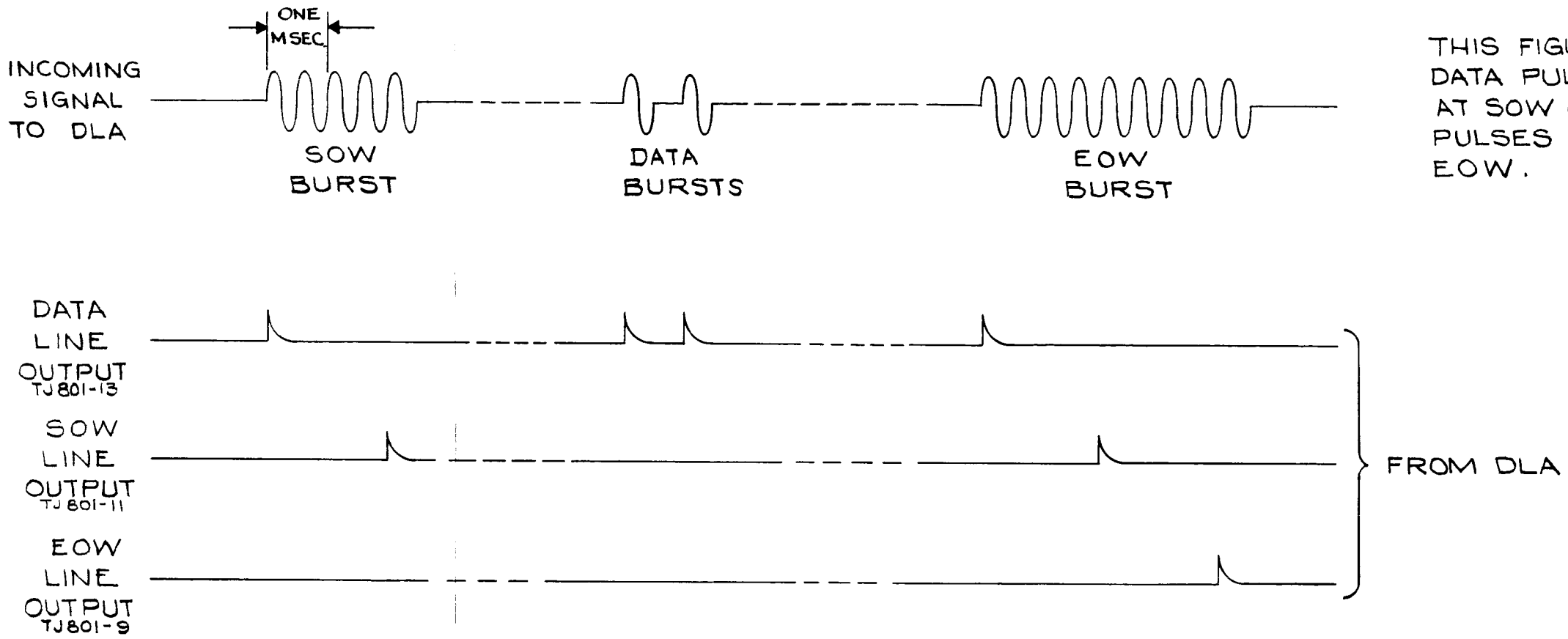
An alternate method of adjusting the oscillator using a frequency counter is acceptable.

2-8.2. Level and Detection - The ideal settings for the level and detection controls

are best determined by examining the detected waveform output, TJ801-48. It is convenient for the remainder of the adjustments to use the delayed sweep feature of the oscilloscope. Using EOW, TJ801-9, as sync, and the delayed sweep, it is possible to examine incoming data occurring over a relatively long period at magnifications where the full sweep displays only a few milliseconds of data, and the scope still maintains sync on a stable source. The level and detection controls, potentiometers R801 and R822, should be adjusted until the detected waveform TJ801-48, has the appearance shown in the Data Line Amplifier Waveform Figure. The detected waveform is nominally a 15 to 20 volt negative pulse. It can be noted that for each bit of data, the ideal waveform produces two negative pulses, each with full amplitude, and squared at the bottom. It is also acceptable and common, due to frequency rolling, to have one of the two pulses of a lesser amplitude. It is unacceptable to have three pulses, specifically because the data one-shot is re-triggered on the third pulse making the output of V805 excessively wide. Proper adjustment, therefore, constitutes the obtaining of maximum amplitude and squareness of the detected signal without detecting three pulses for a data bit. If the adjustments have been made properly, one data pulse will appear at TJ801-13 for each data burst on the input at TJ801-50.

2-8.3. SOW and EOW One-Shots - The SOW and EOW one-shots are variable because the length of the SOW and EOW code bursts depend upon the system in which the Data Line Amplifier is used. These one-shots are normally set for a period that produces a pulse which is 0.5 milliseconds shorter than the incoming code burst for that signal. For example, if SOW is a 2.5 millisecond burst, the SOW one-shot is adjusted for 2 milliseconds. If EOW is a 4.5 millisecond burst, the EOW one-shot is adjusted for 4 milliseconds.

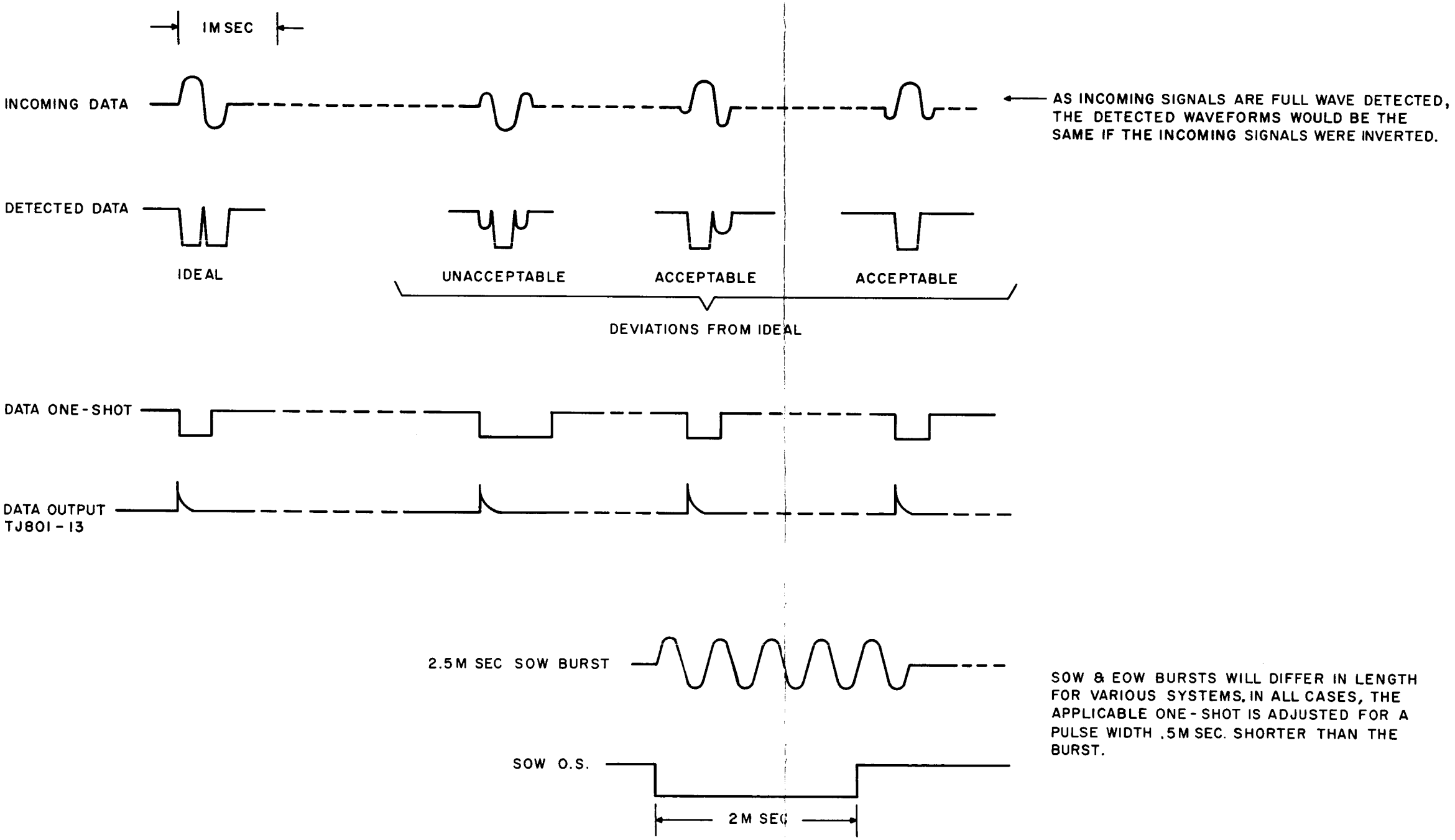
2-8.3.1. To properly adjust the SOW one-shot, using the delayed sweep of the oscilloscope as previously described, synchronize on EOW at TJ801-9 in the Data Line Amplifier. On one trace observe the data input, TJ801-50. On the remaining trace observe the SOW one-shot, TJ801-44. Adjust the time delay of the scope sweep until a SOW burst is seen. It is necessary to observe the one-shot pulse occurring during the SOW burst because during a data burst the SOW one-shot is triggered off by the data one-shot and not allowed to complete its time delay. Adjust potentiometer R849 to set the SOW one-shot for the desired width. Adjust the time delay of the scope until an EOW burst is seen. Observe the EOW one-shot, TJ801-46 and set potentiometer R843 for the desired width.

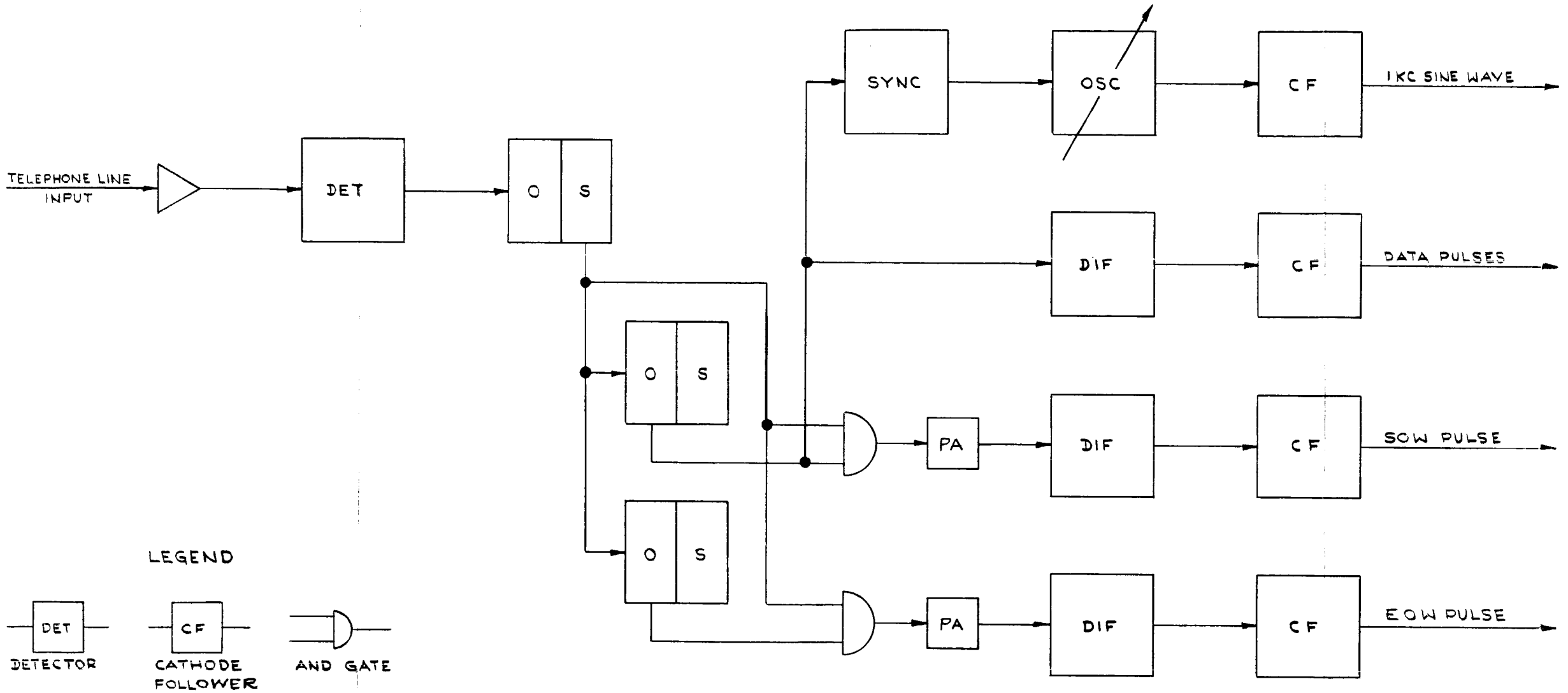


THIS FIGURE SHOWS THAT DATA PULSES ARE OBTAINED AT SOW & EOW - AND SOW PULSES ARE OBTAINED AT EOW.

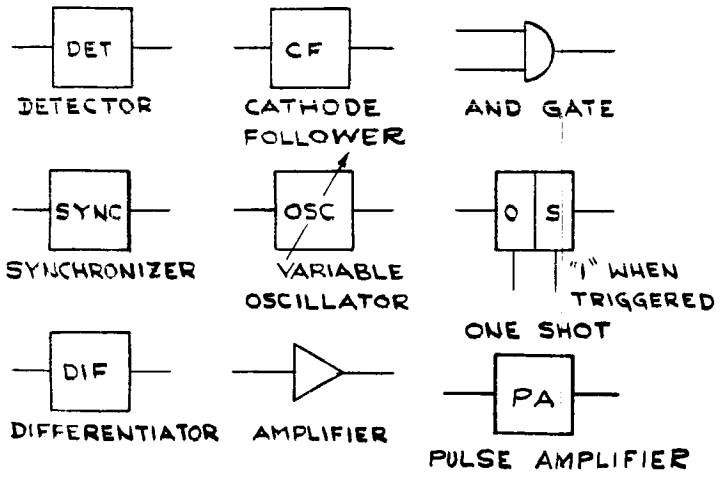
NOTE:

AMPLITUDES NOT DRAWN TO SCALE.
OUTPUT PULSES APPROX. 10 μSEC. WIDE AT HALF AMPLITUDE.
SOW & EOW BURSTS MAY VARY IN LENGTH DEPENDING UPON THE SYSTEM IN WHICH THEY ARE USED.
SOW & EOW OUTPUTS WILL NORMALLY OCCUR .5 M SEC. BEFORE THE END OF BURST.
IN SOME SYSTEMS, SOW AND/OR EOW ARE NOT NECESSARILY USED.

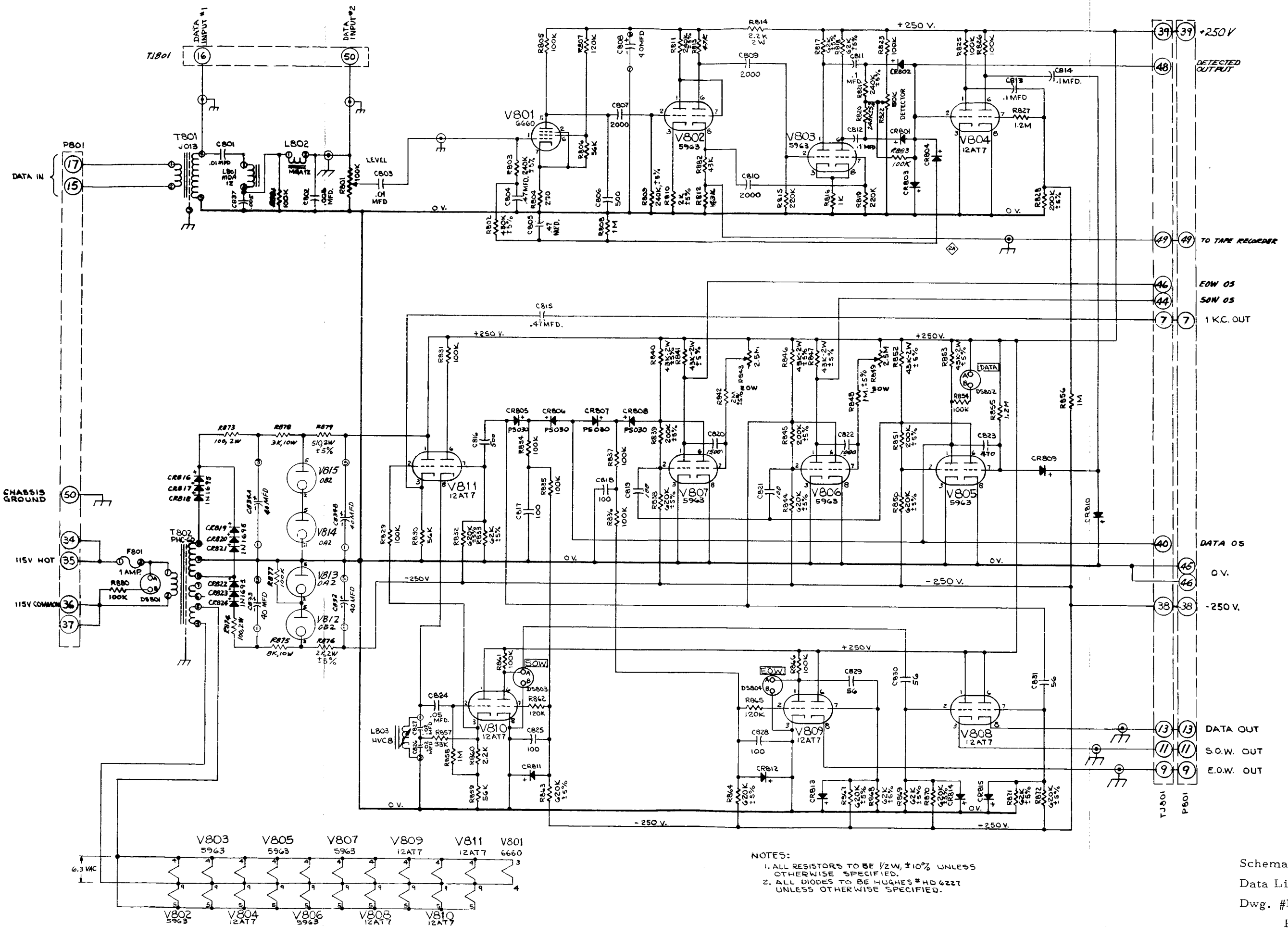

1M SEC
INCOMING DATA
AS INCOMING SIGNALS ARE FULL WAVE DETECTED, THE DETECTED WAVEFORMS WOULD BE THE SAME IF THE INCOMING SIGNALS WERE INVERTED.
DETECTED DATA
IDEAL
UNACCEPTABLE
ACCEPTABLE
ACCEPTABLE
DEVIATIONS FROM IDEAL
DATA ONE-SHOT
DATA OUTPUT
TJ801-13
2.5M SEC SOW BURST
SOW O.S.
2M SEC
SOW & EOW BURSTS WILL DIFFER IN LENGTH FOR VARIOUS SYSTEMS. IN ALL CASES, THE APPLICABLE ONE-SHOT IS ADJUSTED FOR A PULSE WIDTH .5M SEC. SHORTER THAN THE BURST.



LEGEND

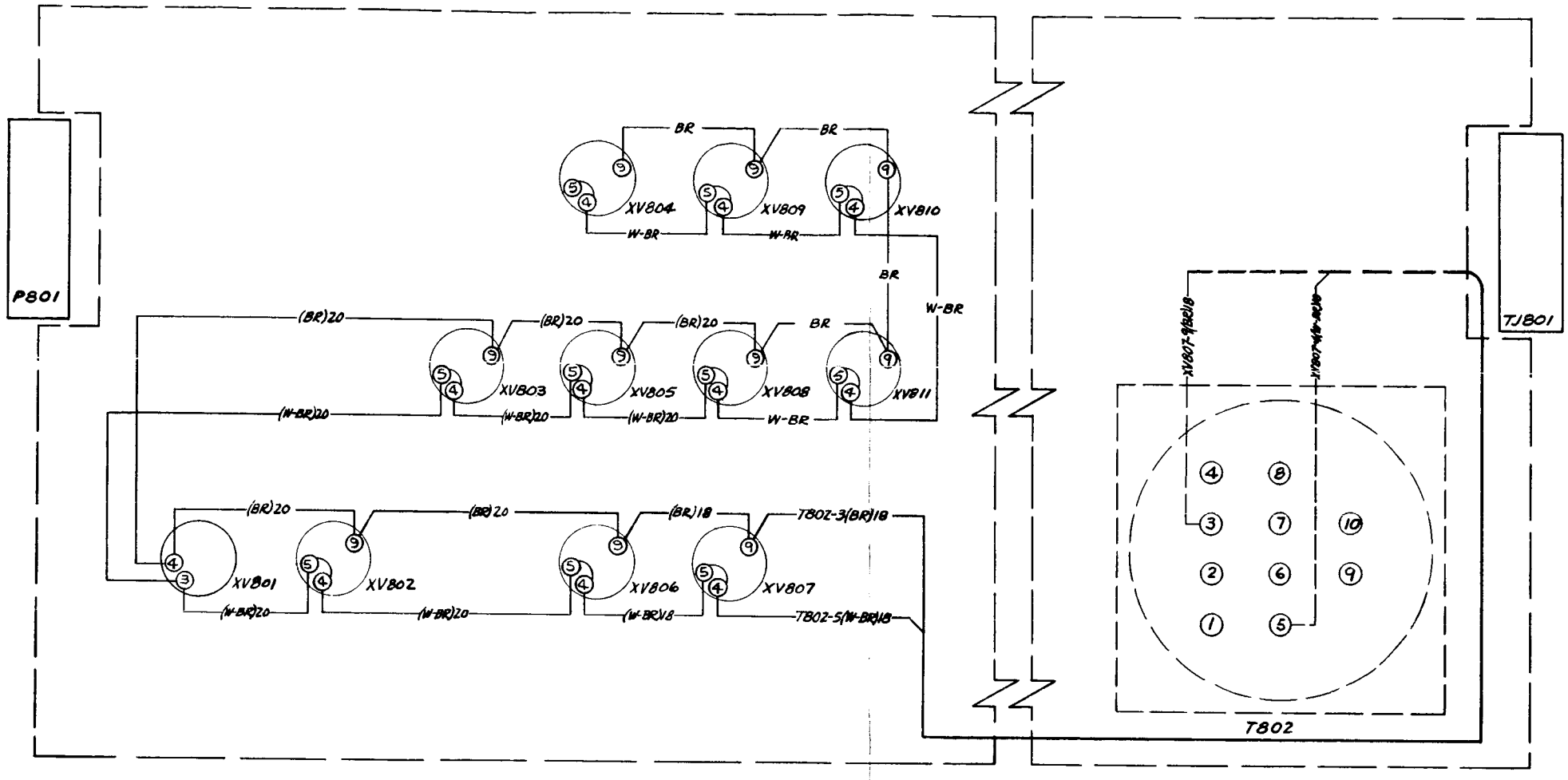


Block Diagram,
Data Line Amplifier,



NOTES:
1. ALL RESISTORS TO BE 1/2W, ±10% UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES TO BE HUGHES #HD 6227 UNLESS OTHERWISE SPECIFIED.

Schematic,
Data Line Amplifier
Dwg. #D71S8A



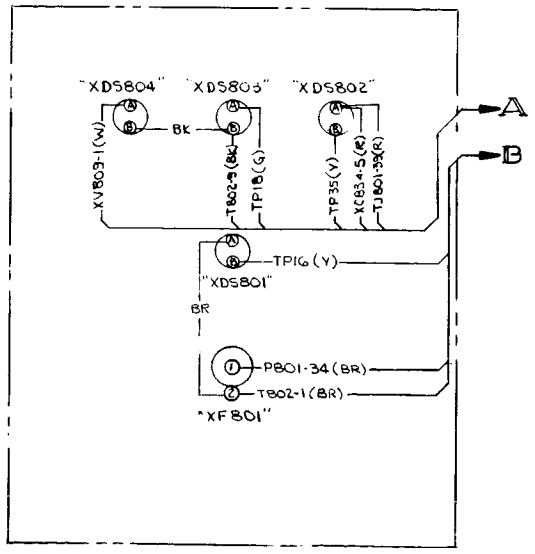
NOTES:

1. ALL WIRES TO BE #22 GA. UNLESS SPECIFIED.
2. ALL FILAMENT WIRES TO BE TWISTED PAIRS.

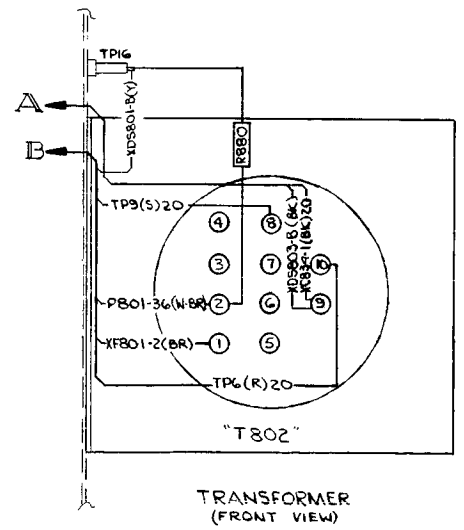
P801			
PIN	DESTINATION	FUNCTION	WIRE
7	TP4	I.K.C. OUT	O
9	XV809-B	E.O.W. OUT	COAX
11	XV808-J	S.O.W. OUT	COAX
13	XV808-B	DATA OUT	COAX
15	T801-2	DATA IN	Y
17	T801-1	DATA IN	BL
34	XF801-1	115 VAC HOT	BR
35		115 VAC HOT	
36	T802-2	115 VAC COM	W-BR
37		115 VAC COM	
45	TP20	0 V.	(BK)20
46	TP21	0 V.	(BK)20
49	TP1A		COAX
50	GND LUG	CHASSIS GND	BK
38	XC832-1	-250 V	S
39	TP19	+250 V	R

JUMPER TERMINALS 34 & 35, 36 & 37, 45 & 46

TJ801			
PIN	DESTINATION	FUNCTION	WIRE
7	TP4	I.K.C. OUT	O
9	XV809-B	E.O.W. OUT	COAX
11	XV808-J	S.O.W. OUT	COAX
13	XV808-B	DATA OUT	COAX
16	T801-4	DATA INPUT #1	COAX
38	XC832-1	-250 V	S
39	XD5802-A	+250 V	R
40	TP25	DATA O.S.	O
44	XV806-1	S.O.W. O.S.	V
47	XV807-1	E.O.W. O.S.	G
48	TP33	DETECTOR OUTPUT	W-V
50	L802-2	DATA INPUT #2	COAX
25	TP1A		COAX



FRONT PANEL
(REAR VIEW)



TRANSFORMER
(FRONT VIEW)

NOTES:
1. ALL WIRE TO BE #22 GA UNLESS OTHERWISE SPECIFIED.
2. ▬▬ DESIGNATES COAX TYPE RG-174/U.
3. GROUND ONE END ONLY OF ALL COAX LEADS.
4. GROUND CENTER POST OF ALL 7 & 9 PIN SOCKETS.
5. FOR FILAMENT WIRING SEE DWG. #C71W8A, SH. #2

Wiring Diagram,
Data Line Amplifier
Dwg. #D71W8A

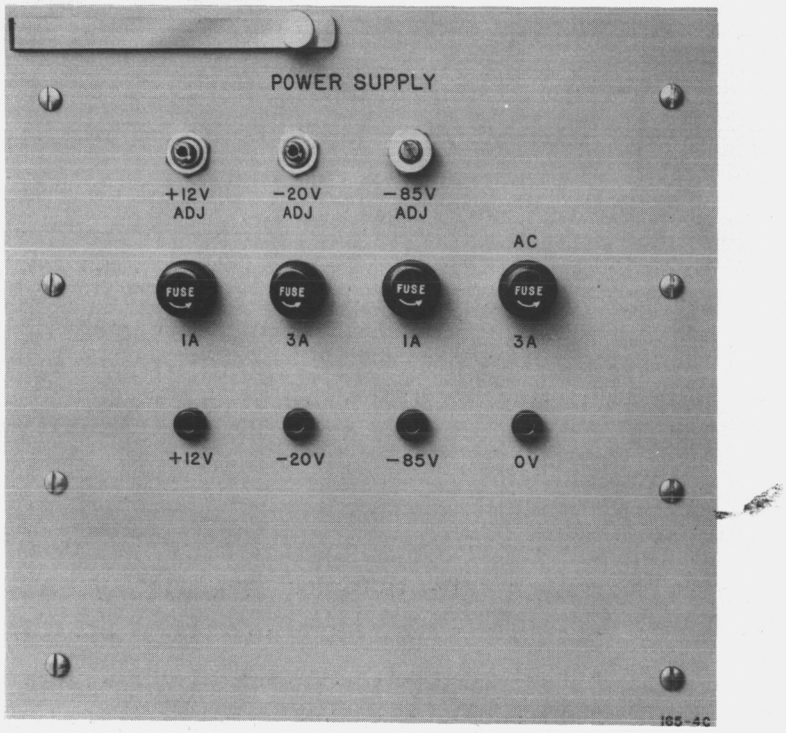
TRANSISTOR POWER SUPPLY
MEC MODEL 165-4 C

1. GENERAL DESCRIPTION

A Milgo type 165-4C Power Supply has three outputs: the first, a +12v, (+1v, -3v) at 1 ampere output; the second, a -20v, (+2v, -6v) at 2 amperes output; and the third, a -65v (±5v) at one ampere output. The -65v supply is stacked on the bottom of the -20v supply, thereby giving an output of -85v. The a-c input of this supply can vary from 100vac to 130vac and from 45 to 60 cycles. The unit is mounted in a standard Milgo slide-type rack and has a front panel 8-3/4 inches high by 8-7/8 inches wide. Its weight is approximately 35 pounds.

2. +12v SUPPLY

2-1. A portion of the output of transformer T401 is rectified by a bridge rectifier CR401 and filtered by resistor R401 and capacitors C401 and C402. The voltage across capacitors C401 and C402 is normally 20v (approximate). Transistor Q401 and resistors R402 and R403 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q401 is decreased so that the IR drop across R402, R403, and Q401 will remain constant producing a constant output voltage. If the input a-c line voltage should increase, the d-c voltage across filtered capacitors C401 and C402 would increase and the effective resistance of Q401 must increase again so that the output voltage will remain constant.



Transistor Power Supply

2-2. The effective resistance of Q401 is controlled by the control section, consisting of transistors Q402, Q403, Q404, and their associated circuitry. Q404 determines whether the output voltage is too high or too low and is followed by power amplifiers Q403 and Q402, which amplify the control signal to the necessary power level for driving Q401. The base voltage of Q404 is referenced from the output of 4.7v zener diode CR402. The emitter voltage of Q404 is determined by the resistor divider network of R413, R414,and R415. The voltage from the wiper of potentiometer R414 is applied to the emitter of Q404.

2-3. As the output voltage increases, the magnitude of the voltage from the wiper of R414 will also increase proportionally. Since the output across zener diode CR402 remains constant as the output voltage increases, the emitter voltage tends to go positive with respect to the base voltage, driving Q404 toward cutoff. As Q404 goes toward cutoff, there is less collector current through R410, so there is less base current in Q403. The emitter current of Q403 decreases, reducing the current through R407 and base current of Q402. With less base current in Q402, the emitter current decreases, reducing the base current of Q401. With less base current, the effective resistance of Q401 will increase. Therefore, the output voltage decreases until Q404 senses the correct relationship between the output voltage and the zener voltage of CR402.

2-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q404 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q404, which increases the base current of Q403, thus increasing the emitter current of Q403 and the base current of Q402. This in turn increases the emitter current of Q402 and the base current of Q401, which reduces the effective resistance of Q401, causing the output voltage to return to its regulated value. Q404 actually is matching the zener voltage to the emitter voltage.

2-5. Since a portion of the output voltage applied to the emitter of Q404 can be varied by potentiometer R414, and the emitter voltage of Q404 is to remain constant, the output voltage must be changed as the resistor R414 is changed. In this manner, the regulated output voltage can be adjusted over a range of +9v to +13v. Capacitor C403 has been added to prevent hunting. Resistors R402 and R403 are included to limit the peak current through transistor Q401 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q401 and Q402. Resistor R404 provides a path for the leakage current of Q402 so that this current does not affect the base current in Q401, allowing Q401 to be more nearly cut off during a light load.

3. -20v SUPPLY

3-1. A second portion of the output of transformer T401 is rectified by bridge rectifier CR421 and filtered by parallel resistors R421A and R421B, and capacitors C421, C422, and C423. The d-c voltage across capacitors C421, C422, and C423 is 30v (approximate). Transistors Q421 and Q422 with their associated resistors R423, R424, and R422 act as a variable resistance element in series with the output load, which can be varied to maintain a constant

output voltage across a variable load. As the load current increases, the effective resistance of Q421 and Q422 is decreased so that the IR drop across R422, R423, R424, Q421, and Q422 will remain constant, producing a constant output voltage.

3-2. If the input a-c line voltage should increase, the d-c voltage across filter capacitors C421, C422, and C423 would increase, and the effective resistance of Q421 and Q422 must increase again to keep the output voltage constant. The effective resistance of Q421 and Q422 is controlled by the control section, consisting of transistors Q423, Q424, and Q425 and their associated circuitry. Transistor Q425 determines whether the output voltage is too high or too low and is followed by power amplifiers Q424 and Q423, which amplify the control signal to the necessary power level for driving Q421 and Q422. The base voltage of Q425 is referenced from the output by a 4.7v zener diode CR422. The emitter voltage of Q425 is determined by a resistor divider network R434, R435, and R436. The voltage from the wiper of potentiometer R435 is applied to the emitter of Q425.

3-3. As the output voltage increases, the magnitude of the voltage from the wiper of R435 will increase proportionally. Since the output across CR422 remains constant as the output voltage increases, the emitter voltage tends to become positive with respect to the base voltage, driving Q425, which is an NPN transistor, toward cutoff. As Q425 goes toward cutoff, there is less collector current through R431, and consequently, there is less base current in Q424. With less base current in Q424, the emitter current of Q424 decreases. With less emitter current in Q424, the current through R428 and the base current of Q423 also decrease. This reduces the emitter current in Q423 and reduces the base current in Q421 and Q422. Less base current in Q421 and Q422 increases their effective resistance, which increases the IR drop across them. Therefore, the output voltage decreases until Q425 senses the correct relationship between the output voltage and the zener voltage of CR422.

3-4. Conversely, if the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q425 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q425, increasing the base current of Q424, which in turn increases the emitter current of Q424 and the base current of Q423. This, in turn, increases the emitter current of Q423 and the base current of Q421 and Q422, reducing the effective resistance of Q421 and Q422, and causing the output voltage to return to its regulated value. Transistor Q425 is actually matching the zener voltage to the emitter voltage.

3-5. Since a portion of the output voltage applied to the emitter of Q425 can be varied by potentiometer R435, and the emitter voltage of Q425 is to remain constant, the output voltage will have to be changed as the resistor R435 is changed. In this manner, the regulated voltage of this supply can be adjusted from -14v to -22v. Capacitors C425 and C424 provide feedback for stabilization purposes.

3-6. Resistors R423 and R424 serve two functions. First, they force the collector current of Q421 and Q422 to balance. Since the bases are tied in common, if one transistor conducts

more than the other, the higher IR drop in their associated resistor would tend to reverse bias the transistor with the most current and, in this manner, force the currents to balance. Second, if the output supply is shorted, resistors R422, R423 and R424 limit the peak current through Q421 and Q422 to a safe value while fuse F402 is melting. Resistor R425 provides a path for the leakage current of Q423 so that this leakage current does not affect the base current in Q421 and Q422. This allows Q421 and Q422 to be more nearly cut off during a light load.

4. -65v SUPPLY

4-1. A third portion of the output of transformer T401 is rectified by a bridge rectifier CR441 and filtered by resistor R441 and capacitors C441 and C442. The voltage across capacitor C441 and C442 is normally 75v (approximate). Transistor Q441, and resistors R442 and R443, act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q441 is decreased so that the IR drop across R442, R443, and Q441 will remain constant, producing a constant output voltage. If the input a-c line voltage increases, the d-c voltage across filtered capacitors C441 and C442 will increase and the effective resistance of Q441 must increase again so that the output voltage will remain constant.

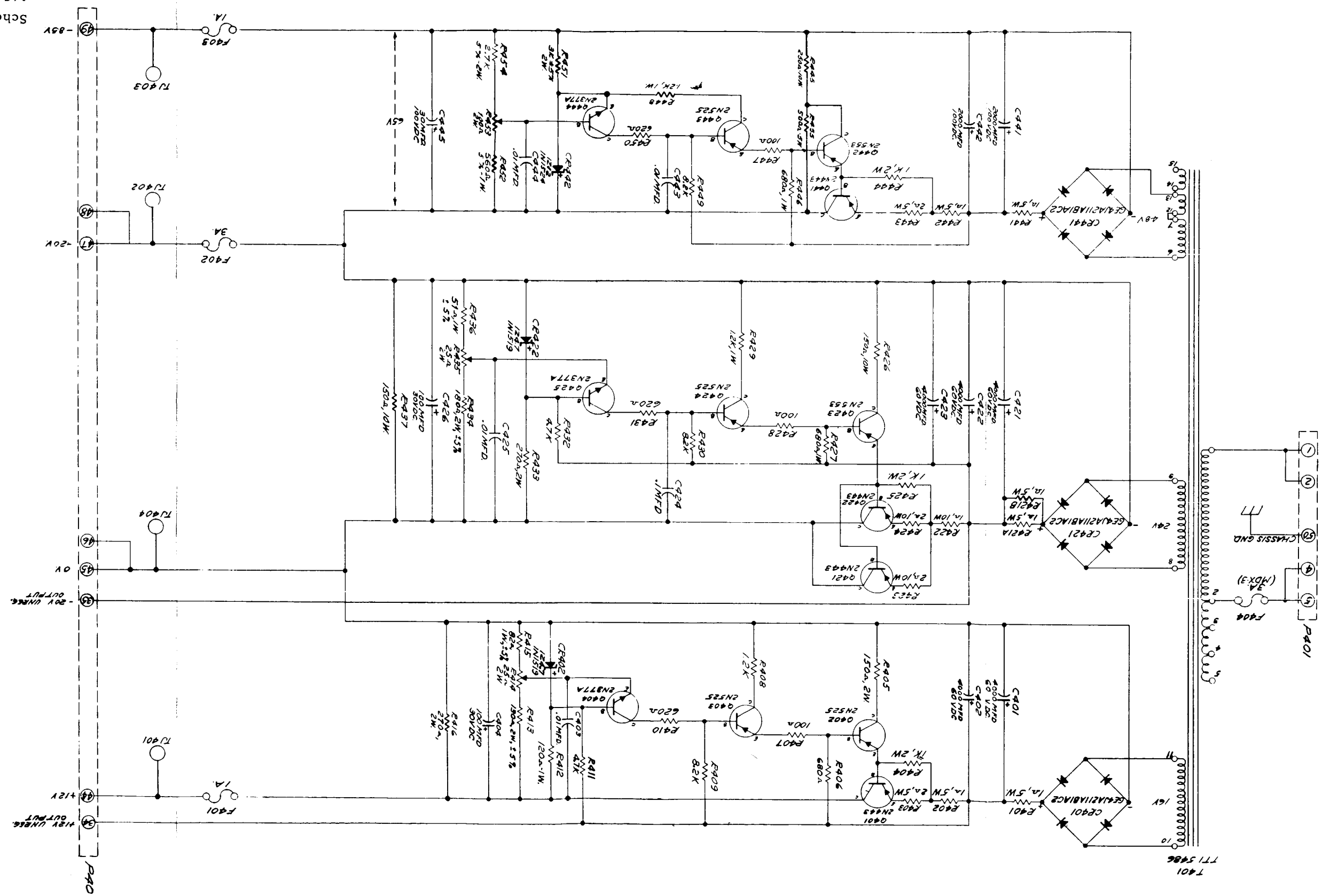
4-2. The effective resistance of Q441 is determined by the control section, consisting of transistors Q442, Q443, and Q444 and their associated circuitry. Q444 determines whether the output voltage is too high or too low and is followed by power amplifiers Q443 and Q442. These amplify the control signal to the necessary power level for driving Q441. The emitter voltage of Q444 is referenced from the output by a 12v zener diode CR442. The base voltage of Q444 is determined by the resistor divider network of R452, R453, and R454. The voltage from the wiper of potentiometer R453 is applied to the base of Q444. The zener is referenced from the positive side of this supply to reduce the emitter-to-collector voltage of Q443 and Q444 to less than 25v.

4-3. As the output voltage increases, the magnitude of the voltage from the wiper of R453 will also increase proportionally. Since the output across zener diode CR442 remains constant as the output volts increase, the base voltage tends to become negative with respect to the emitter voltage, driving Q444 toward cutoff. As Q444 goes toward cutoff, there is less collector current through R450 and less base current in Q443. The emitter current of Q443 decreases, reducing the current through R447 and the base current of Q442. With less base current, the Q442 emitter current decreases, reducing the base current of Q441. With less base current, the effective resistance of Q441 increases. Therefore, the output voltage decreases until Q444 senses the correct relationship between the output voltage and the zener voltage of CR442.

4-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the base of Q441 also decreases, tending to make the base more positive

with respect to the emitter. This increases the collector current of Q444, increasing the base current of Q443, and increasing the emitter current of Q443 and the base current of Q442. This in turn increases the emitter current of Q442 and the base current of Q441, reducing the effective resistance of Q441, and causes the output voltage to increase and to return to its regulated value. Q444 is actually matching the zener voltage to the base voltage.

4-5. Since a portion of the output voltage applied to the base of Q444 can be varied by potentiometer R453, and the base voltage of Q444 is to remain constant, the output voltage will have to be changed as the resistor R453 is changed. In this manner, the regulated output voltage can be adjusted over a range of -60v to -70v. Capacitors C443 and C444 have been added to prevent hunting. Resistors R442 and R443 are included to limit the peak current to transistor Q441 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q441. Resistor R444 provides a path for the leakage current of Q442 so that this current does not affect the base current in Q441. This allows Q441 to be more nearly cut off during a light load. This -65v power supply is stacked on the bottom of the -20v supply giving a combined output of -85v.


-85V
-20V
+12V
-20V UNREG. OUTPUT
+12V UNREG. OUTPUT
0 V
51V
48V
24V
16V
10V
CHASSIS GND
F403 7A.
F402 3A.
F401 7A.
TJ403
TJ402
TJ404
TJ401
P40
P401
T401 TTI 5486
F404 3A (MDX.3)
CR402
CR422
CR421
CR441
Q402 2N3771A
Q425 2N3771A
Q404 2N3771A
Q424 2N3771A
Q403 2N5251
Q423 2N5251
Q405 2N5251
Q425 2N5251
Q401 2N4443
Q421 2N4443
Q441 C144A3
Q442 2N5339
Q422 2N5339
Q402 2N5339
Q423 2N5339
Q403 2N5339
Q424 2N5339
R441 1Ω, 5W
R442 1Ω, 5W
R443 2Ω, 5W
R444 1K, 2W
R447 100Ω
R448 680Ω, 1/4W
R449 12K, 1W
R450 620Ω
R445 560Ω, 1/4W
R446 2.7K, 2W, 5%
R447 3.3K, 2W
R452 1.8K, 1/4W, 5%
R453 560Ω, 1/4W, 5%
R454 2.2K, 1/4W, 5%
R455 51Ω, 1/4W, 5%
R456 270Ω, 2W
R457 150Ω, 1W
R458 1.8K, 1/4W, 5%
R431 620Ω
R428 100Ω
R429 12K, 1W
R426 150Ω, 1W
R427 680Ω, 1/4W
R430 82K
R432 47K
R433 MET. FILM 150Ω, 1/4W, 1%
R421A 1Ω, 5W
R421B 1Ω, 5W
R422 1Ω, 10W
R423 2Ω, 10W
R424 2Ω, 10W
R425 1K, 2W
R410 620Ω
R407 100Ω
R408 12K
R405 150Ω, 2W
R406 680Ω
R409 82K
R411 47K
R412 120Ω, 1W, 1%
R413 100Ω, 2W, 1%
R414 2.2K, 1W, 1%
R415 2.2K, 1W, 1%
R416 270Ω, 2W
R404 1K, 2W
C441 2000 MFD 100 VDC
C442 2000 MFD 100 VDC
C421 2000 MFD 100 VDC
C422 2000 MFD 100 VDC
C401 2000 MFD 100 VDC
C402 2000 MFD 100 VDC
C423 2200 MFD 50 VDC
C403 .01 MFD
C424 .1 MFD
C425 .01 MFD
C426 180 MFD 50 VDC
C404 2200 MFD 50 VDC
C445 2200 MFD 100 VDC
C446 .01 MFD
C447 .01 MFD
C448 .1 MFD
CR441 (GE A2/A2/1A/BI/AC2)
CR421 (GE A2/A2/1A/BI/AC2)
CR401 (GE A2/A2/1A/BI/AC2)
CR422 1N5194
CR402 1N5194
CR403 1N5194
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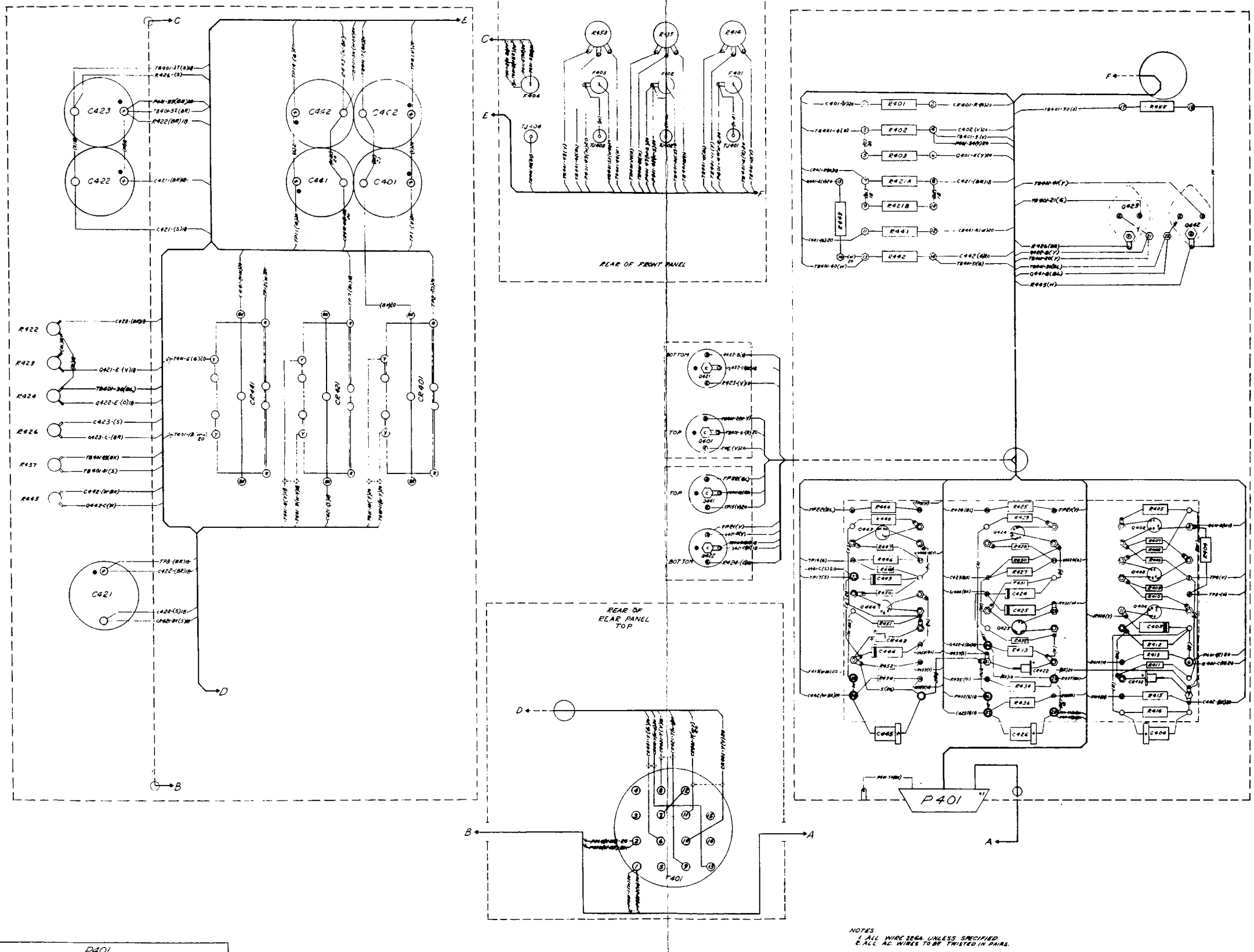


P401							
PIN	DEST.	FUNCTION	WIRE	PIN	DEST	FUNCTION	WIRE
1	TB401-1	AC INPUT	(W) 20	41			
2	TB401-1	AC INPUT	(W) 20	42			
3				43			
4	F404	AC INPUT	(BR) 20	44	F401	+12 V	(W-R) 20
5	F404	AC INPUT	(BR) 20	45	TB401-25	0 V	(BK) 20
6				46	TB401-25	0 V	(BK) 20
7				47	F402	-20 V	(W-S) 20
8				48	F402	-20 V	(W-S) 20
49	[illegible]	[illegible]	[illegible]	49	F403	-8.8 V	(W) 20
50	CHASSIS	CHASSIS GND	(BK)	50	CHASSIS	CHASSIS GND	(BK)

NOTES:
1. ALL WIRE 22GA. UNLESS SPECIFIED.
2. ALL AC WIRES TO BE TWISTED IN PAIRS.

Wiring Diagram
165-4C Power Supply
Dwg. #E165W46

MAGNETIC CORES

1. GENERAL

A component commonly used in digital data handling equipment is a magnetic core. The term magnetic core is usually applied to a small torroid composed of magnetic material which has high permeability and also high retention. This material will have what is called a square hysteresis loop, shown in Point A, Figure MN-1. Because of this square hysteresis loop, there are two stable energy states, which make the cores adaptable to digital circuits. Magnetic cores are commonly used for shift registers, "and" gates, "or" gates, and other logic circuits, in addition to their use as blocking oscillator transformers.

2. THEORY OF OPERATION

2-1. GENERAL

a. The action of a magnetic core can best be described by referring to the drawing of the hysteresis loop (Figure MN-1). The magnetomotive force, or ampere-turns, applied to the winding of a core is measured along the X axis. Magnetic flux density (gausses), or flux lines per square centimeter, is being measured along the Y axis. Once a core has been magnetized and had this magnetization reversed several times, the relationship between flux density and magnetomotive force is described by the hysteresis loop in Figure MN-1.

b. With no current going through any of the core windings, the flux density will be either at point D or at point H, depending upon the direction in which the core has most recently been saturated. If the core is assumed to be at point D on the hysteresis loop and ampere-turns are applied in the negative direction, the relationship between the flux density and the magnetomotive force will follow the line DE. If additional ampere-turns are applied in the negative direction, the core will go on to condition F, at which point saturation has occurred and additional ampere-turns of magnetomotive force will result in only a minor increase in flux level to point G.

c. If the current through the windings is now removed, the core will return to point H on they hysteresis loop. Even though there are no ampere-turns, there is still a flux density proportional to OH in the core. The characteristics of the core material are such that this

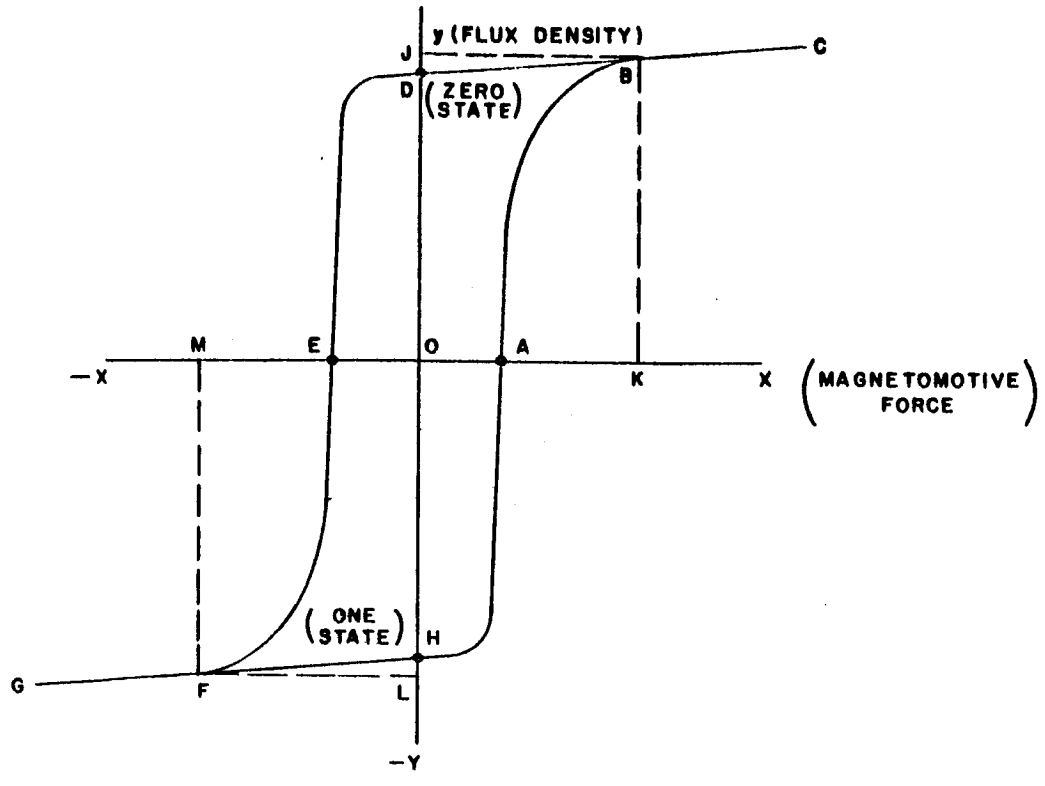


Figure MN-1. Square Hysteresis Loop

flux density will remain indefinitely as though it were a permanent magnetic. If the direction of current in the winding is reversed, positive ampere-turns are applied. This will move the condition of the core from H to A and on to B, at which point the core is now saturated in the positive direction and additional ampere-turns of magnetomotive force will cause very little change in flux density to point C. When the current in the coil is removed, the core will now go from C to D, where it will remain indefinitely until driven again.

d. The net change in flux, when going from a negative quiescent state to plus saturation, is proportional to HJ. It should be noted that other windings on the magnetic core will sense this change in flux and will generate a voltage proportional to the number of turns and the rate of change of flux. Figure MN-2 shows a simple magnetic core with three windings on it. If positive ampere-turns are then applied to winding No. 1, the core condition effectively goes from D to B. Since the hysteresis loop is very square, the change in flux during this time (proportional to DJ) is very small when compared to HJ. As a result, the voltage generated in coil No. 2 will be very small at this time.

e. If negative ampere-turns are again applied so that the core goes from D to E to F, the

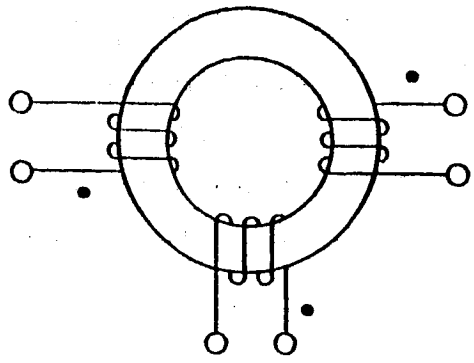


Figure MN-2. Simple Magnetic Core

change in flux will be proportional to DL. The voltage generated in winding No. 2 will now be equal in magnitude, but opposite in polarity, to the voltage generated in that winding when the core went from H to B. These pulses can be separated with diodes and used for different purposes in logic circuits. The two stable states, D and H, are referred to as the "0" state and the "1" state respectively.

2-2. MN11 MAGNETIC CORE

a. A Milgo MN11 magnetic core has four windings and associated components designed specifically for shift register application (Figure MN-3). Pin 7 is connected to a -25v supply. The core drive pulse, applied to pin 1, travels from -25v to approximately zero volts and return, with a rise time no greater than 5 microseconds and a fall time no greater than 10 microseconds. The pulse width must be at least 10 microseconds at 50 percent of measured points, but is normally approximately 40 microseconds wide.

b. This positive going pulse applied to pin 1 results in ampere-turns driving the core beyond positive saturation (Point C in Figure MN-1). When the core drive pulse has passed, the core is left in state D, which is defined as "O" state. The voltage at pin 8 is normally maintained at -25v but is raised to approximately -16v to insert a "1" into the core. It can be seen that the current in the input winding, as a result of a positive going pulse applied to pin 8, will magnetize the core in an opposite direction to that of the drive pulse. The state of the core will go from D to G on the hysteresis loop (Figure MN-1), and when the input pulse is passed, the core remains at H, which is defined as a "1" state.

c. When the next drive pulse occurs, the flux will travel from point H to Point C, and

transformer action of the core and windings will result in a positive pulse being generated at the dot end of all four windings. This positive pulse will be approximately 9v in magnitude with a rise time of approximately 6 microseconds. Once the core has gone from negative saturation to positive saturation, there will be no more flux change even though the drive pulse is still present, and no additional voltage is generated in the windings. This switching time, which takes place in approximately 6 microseconds, determines the width of the pulse generated by the windings.

d. The 9v pulse generated in the advance winding causes diode CR3 to conduct, and will charge capacitor C3 to approximately -16v. After the core has switched to positive saturation, the voltage at pin 6 will revert to -25v. Diode CR3, however, prevents capacitor C3 from discharging through the advance winding, so the charge is held on C3 until it discharges through an external load.

e. During a core drive pulse, the voltage at pin 2 jumps from -25v to approximately zero volts because of the IR drop in R1 caused by the shift current. With pin 2 at approximately zero volts, diode CR2 will be reverse biased and no current can flow from pin 8 through CR2 and the input winding. After the core drive pulse has passed, the -16v charge on one CR3 can now discharge through CR2 and the input windings of the next core, driving it to the "1" state. A "1" can be inserted by raising pin 8 to -21v, or more positive. It should be pointed out that a "1" can also be inserted through pin 3, or by applying a pulse to pin 5, which becomes approximately 8v positive with respect to pin 4. If there is no "1" inserted between core drive pulses, the next core drive pulse will drive the core from point D to point C on the hysteresis loop, resulting in a very small change in flux density. This will result in a very small voltage being generated in the windings (approximately 0.5v), giving a signal-to-noise ratio of approximately 18 to 1.

f. It should be noted that energy transferred to a load while shifting out a "1" comes from the core driver and not from the core. The energy in the core merely allows energy to be transferred to the output winding while the core is acting as a transformer. The Milgo MN11 operates equally well on a power supply voltage of -20v instead of -25v as described.

2-3. SHIFT REGISTERS

a. When connected to form a shift register, MN11 cores are connected as shown in Figure MN-3. If a positive going pulse is applied to pin 8 of the first core, a "1" will be inserted into that core. During the next core drive pulse, all of the cores will be pulsed simultaneously, since they are connected in parallel. The resultant 9v pulse from the advance winding

of the first core will charge the capacitor in the first core to approximately -16v. When the first core has switched from minus saturation to plus saturation, there will no longer be any voltage generated in the advance winding. CR3 of the first core will prevent the capacitor from discharging through the advance winding, however, and CR2 in the second core prevents this capacitor from discharging through the input winding of the second core. CR2 is reverse biased because of the IR drop in the resistor of the second core caused by the shift current.

g. When the shift pulse has passed, the pin 2 voltage of the second core will go back to -25v and the capacitor in the first core may now discharge through the input winding of the second core. The resultant current through the input winding is sufficient to drive the second core from point D to point G on the saturation curve, so that when C3 is completely discharged, the second core will be in a "1" state. While this second core was being switched from plus saturation to minus saturation, flux linkages were changing in all of the windings of this core, with the result that a voltage was generated in all of these coils with the dot end of the winding negative. Diode CR1 will prevent any current flow in the drive winding as a result of the generated voltage, and the diode CR3 will prevent any current flow in the advance winding as a result of this generated voltage.

h. During the next core drive pulse, core 2 is switched from minus saturation to plus saturation, resulting in the output capacitor of the second core being charged. After the second core drive pulse, the discharge current from this capacitor will insert a "1" into the third core and so on to the last one. Since both ends of the auxiliary winding are brought out, the auxiliary winding may be used to generate either a positive going or negative going 9v pulse. This auxiliary pulse will be approximately 9v in magnitude, with a rise time of six microseconds and a fall time of approximately one half microsecond. In addition, the auxiliary winding can be used to insert "1's" into the core by applying a suitable positive pulse to pin 5 or a suitable negative pulse to pin 4. Pins 2, 3, and 6 are brought out for additional flexibility in adapting the MN11 core to logic circuits.

2-4. BLOCKING OSCILLATORS

a. The use of transformers for blocking oscillators is common and widely understood. It is also possible to use a square loop magnetic core as a blocking oscillator transformer with some desirable results in control of pulse width. Figure MN-4 shows the connections of either an MN12 or an MN13 as used in a blocking oscillator.

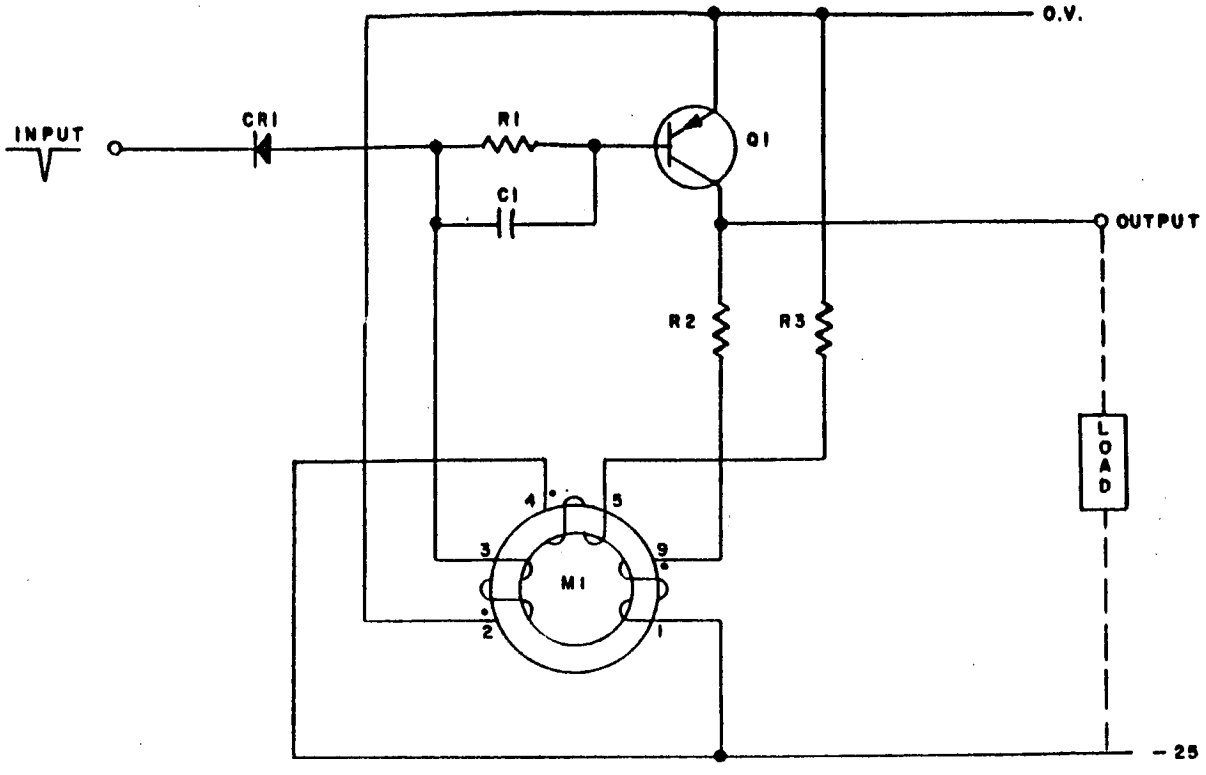


Figure MN-4. Blocking Oscillator (MN12 or MN13)

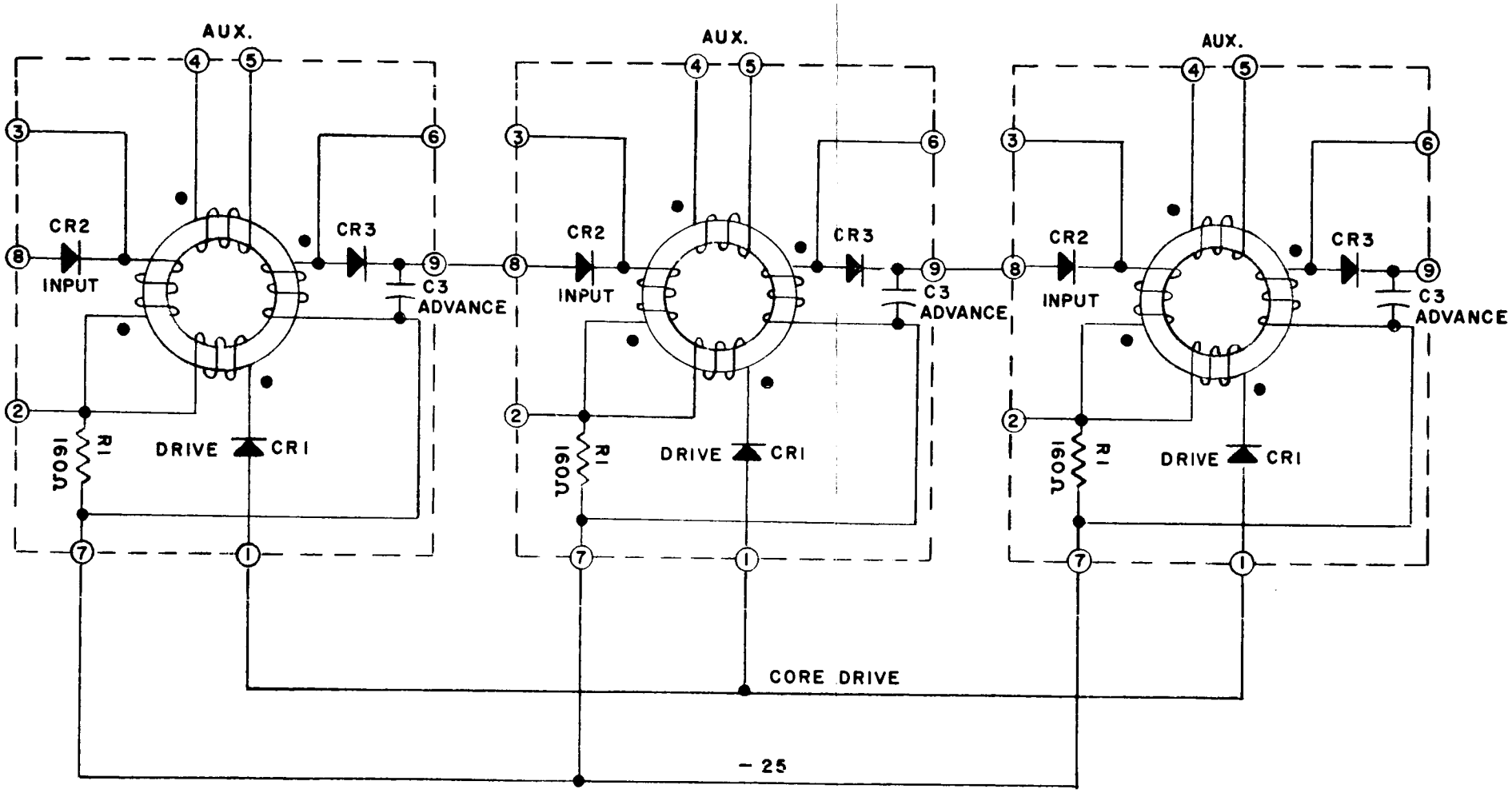
b. The 9-1 winding is the collector winding and could be compared to the primary winding of a transformer. The 2-3 winding is the feedback winding and could be compared to the secondary winding of a transformer. The 4-5 winding is the reset winding and has no counterpart in a conventional transformer. The reset winding is so connected that the current through the reset winding will drive the core into negative saturation. The transistor will normally be cut off, but when triggered by a negative pulse at the input, will go into conduction. The resulting collector current applies positive ampere-turns to the core and the flux moves from H toward A and B. The resulting flux change in the core is sensed by the feedback winding and a voltage is generated, making pin 3 negative. This negative going voltage is applied to the base of the transistor and drives the transistor into heavier conduction.

c. As the transistor conducts more heavily, the rate of change of flux increases, resulting in an even more negative voltage being applied to the base of the transistor. This feedback very quickly saturates the transistor (approximately one microsecond), but the collector current is limited by resistor R2 and the voltage generated in the collector winding of the core. As long as the core is still in the process of switching from minus saturation to plus

saturation, the core and its windings act as a transformer and the feedback winding continues to drive the transistor into saturation. When the core has finally reached saturation (B on hysteresis curve, Figure MN-1), additional ampere-turns from the collector winding will no longer result in a change of flux and no additional voltage will be generated in the feedback winding. This removes the drive to the transistor, which immediately cuts off, removing the ampere-turns from the collector winding.

d. Current through resistor R3 and the reset winding now starts to apply ampere-turns in the negative direction again and drives the core from position D to F. This results in a reversal of flux in the core, which reverses the voltage generated in the feedback winding. Pin 3 now becomes slightly positive, insuring a rapid cutoff of the transistor. Since the duration of the output pulse depends on the time it takes to switch the magnetic core, the pulse width depends on the core used and is relatively independent of the load on the blocking oscillator.

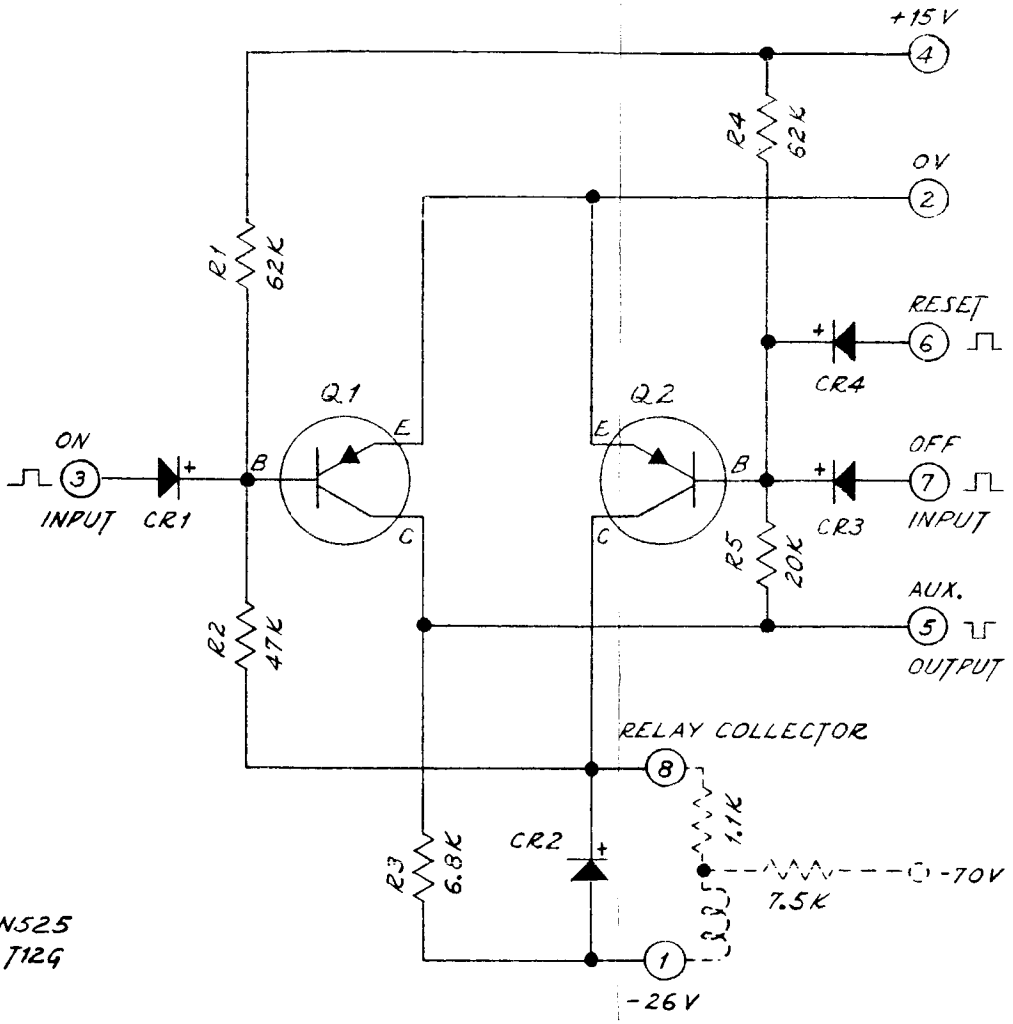
e. Two blocking oscillator cores are used in Milgo equipment: an MN12 and an MN13. The MN12 will cause a pulse approximately 10 microseconds wide to be generated by the blocking oscillator, while the MN13 will cause a pulse approximately 40 microseconds wide to be generated. It takes approximately 30 microseconds to reset an MN12 core and approximately 80 microseconds to reset an MN13 core.


AUX.
CR2
INPUT
CR3
C3
ADVANCE
160Ω
R1
DRIVE
CR1
CORE DRIVE
- 25

TN 28
RELAY DRIVING FLIP-FLOP

A TN28 is a bistable flip-flop which can be used for driving a relay coil or other loads of 500 ohms or more. The external load (shown on the schematic diagram in phantom between pins 8 and 1) is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" or "0" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "on" or "1" condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize. Assuming that Q1 is saturated, then its collector is approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -.05 volts; so the current through resistor R1 is approximately 0.25 milliamps. The current through the series combination of R2 and the external load resistor, which may very from 500 ohms to 5K, varies from 0.53 to 0.48 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so this condition is a stable one. The input voltages at pins 3, 6 and 7 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Now resistors R1 and R2 are connected from +15 to 0 volts and hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This, then, is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR2 is included to suppress the voltage of an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cutoff, the relay coil is de-energized. However, the inductance of the relay coil attempts to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and so does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil

and eliminating the voltage spike. Although the description of operation of this network has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.



Q1, Q2 - 2N525
CR1-CR4 - T12G

Schematic,

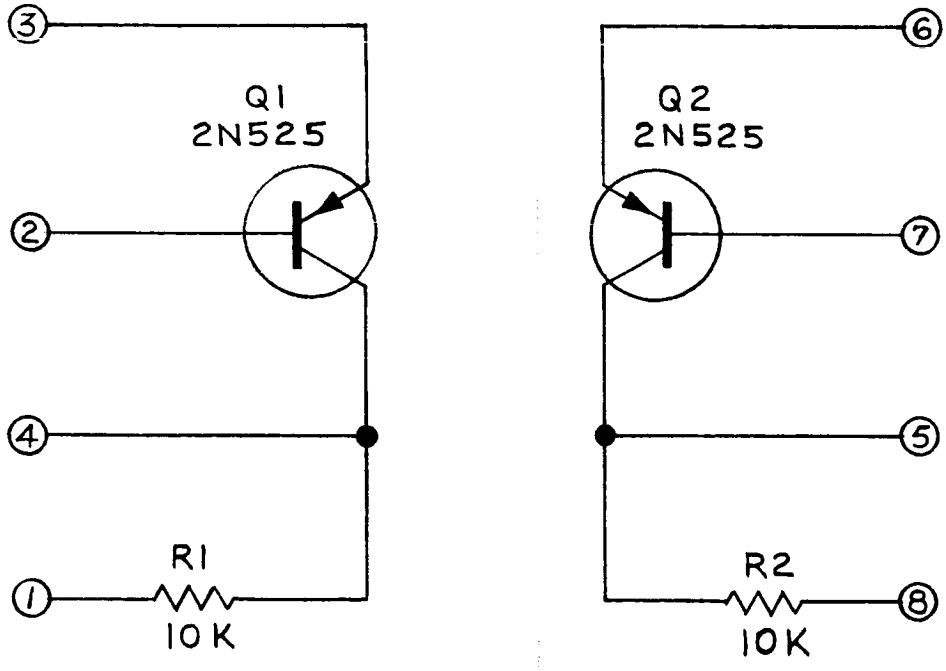
TN28 Relay Driving Flip-Flop

Dwg. #A103S28A

TN 57
DUAL PULSE AMPLIFIER

The TN57 contains two PNP transistors connected as two independent conventional amplifiers. Only one of these will be discussed since the other is identical to it. As normally used, a supply voltage is connected to pins 3 and 1 with the plus side on pin 3. Pin 2 will be the input and pin 4 the output. As long as pin 2 is more positive than pin 3 the transistor is cut off and the voltage at pin 4 will be the same as the voltage at pin 1. When pin 2 is approximately 0.5 volts negative with respect to pin 3 the transistor will saturate and the voltage at pin 4 will go positive until it saturates, approximately 0.25 volts more negative than the emitter. Caution must be used to connect an external base resistor in series with pin 3 to prevent damage to the transistor. The value of the external base resistor is dependent upon how negative the driving voltage goes and upon the external load that is connected to pin 4. To insure saturation the base current should be at least 1/20th of the collector current.

The TN57 may also be used in a variety of applications by the addition of external components.



Schematic

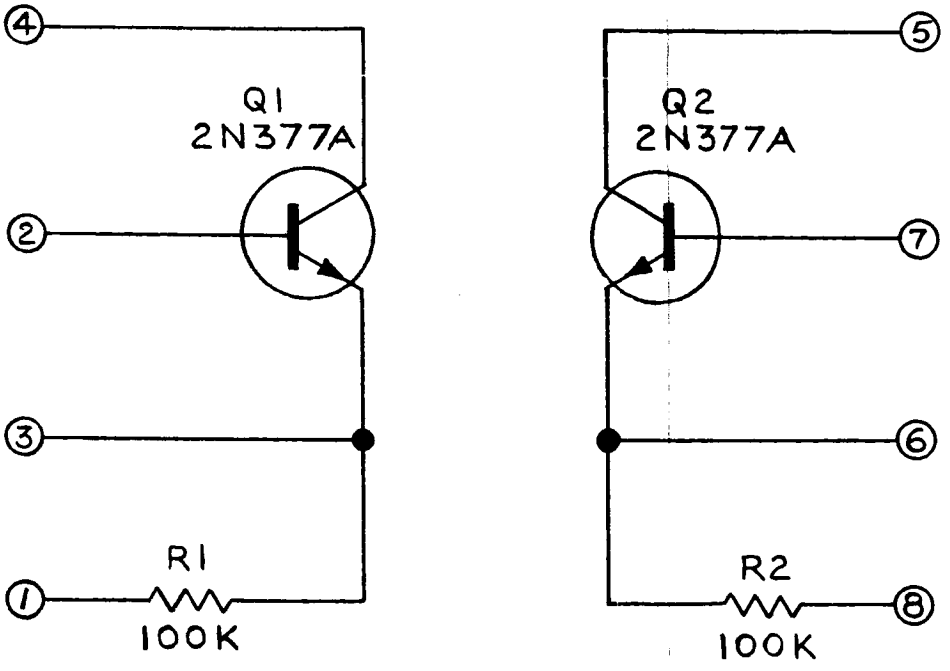
TN57 Dual Pulse Amplifier

Dwg. #A103S57A

TN 58
DUAL EMITTER FOLLOWER

A TN58 consists of two NPN transistors connected as independent emitter followers. As normally used, a supply voltage is connected to pins 4 and 1 with the plus side on pin 4. As the voltage at pin 2 is varied, between the voltages at pins 4 and 1, the transistor will conduct and the voltage at the emitter, pin 3, will be approximately 0.4 volts more negative than the voltage at pin 2. Because of the power gain of the transistor a lower impedance load can be driven from pin 3 than could have been driven from the signal applied to pin 2.

The TN58 may also be used in a variety of applications by the addition of external components.



Schematic

TN58 Dual Emitter Follower

Dwg. #A103S58A

TN 79
RELAY DRIVING FLIP-FLOP

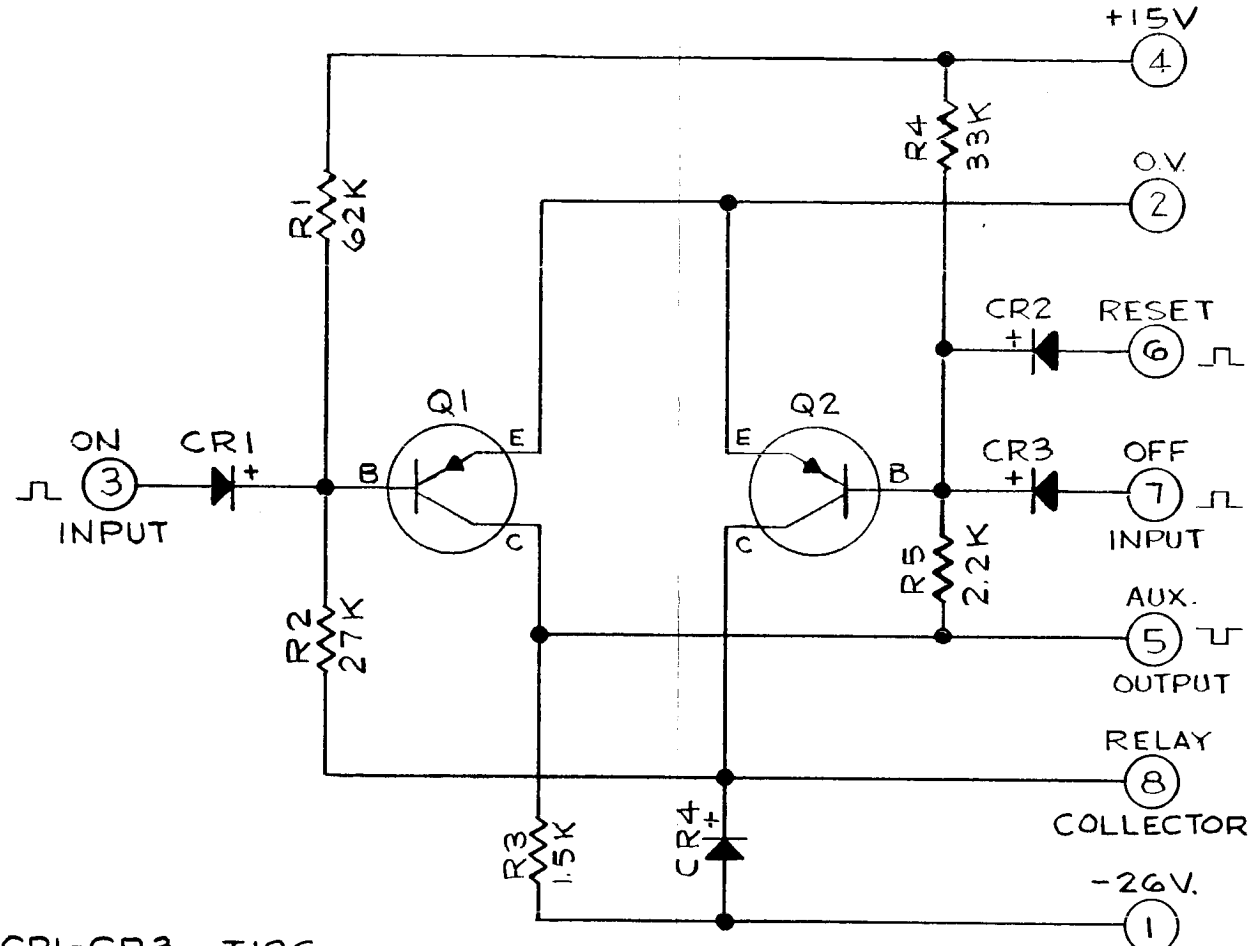
A TN79 is a bistable flip-flop which can be used for driving a relay coil (or other load) of 200 ohms or more. The external load is connected between pins 8 and 1. The network is normally said to be in the "Off" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "On", or "1", condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize.

If we assume that Q1 is saturated, then its collector is at approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter of Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base will be at approximately -0.5 volts, and the current through resistor R1 is approximately 0.25 ma. The current through the series combination of R2 and the external load resistor, which may vary from 300 ohms to 3K, will vary from 0.93 to 0.85 ma. The difference between the currents in R1 and in R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition; therefore, that condition is a stable one.

The input voltages at pins 3, 6, and 7 must be negative during quiescent conditions. The flip-flop may be turned "On" by raising the voltage at pin 3 to a positive value so the diode CR1 conducts, raising the base voltage of Q1 to a positive value. The input pulse will be loaded slightly and cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Resistors R1 and R2 are now connected from +15 volts to 0 volts, and hold the base of Q1 at approximately +4.5 volts, keeping Q1 in a cut off condition after the input pulses pass. This is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition.

Diode CR2 is included to suppress the external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cut off, the relay coil is de-energized. However, the inductance in the relay coil attempts to maintain the current through the coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by

the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil and eliminating the voltage spike. This network will operate on a lower supply voltage, such as +12 volts and -20 volts.



CR1-CR3 - T12G
CR4 - 1N1692
Q1, Q2 - 2N525

Schematic,

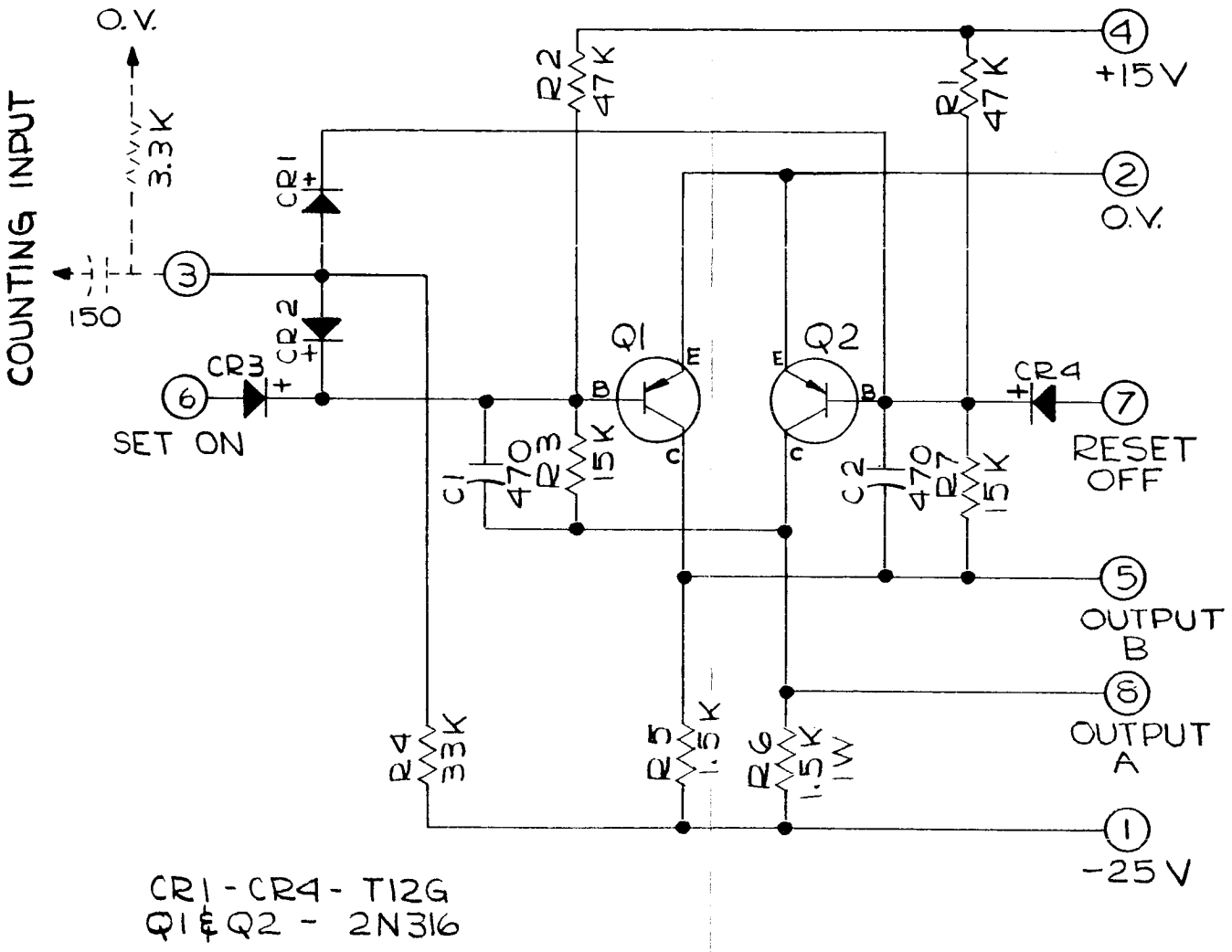
TN79 Relay Driving Flip-Flop

Dwg. #A103S79A

TN 90B
BALANCED FLIP-FLOP AND DIVIDER

The TN90B is a bistable balanced flip-flop. An auxiliary input (pin 3) allows the network to be used as a divider in a counter.

The network is defined as being in the "0" state when Q1 is saturated and Q2 is off and in the "1" state when the reverse is true. Assume that Q1 is saturated ("0" state) then the collector voltage of Q1 will be approximately 0 volts and resistor divider, R1 and R7, will maintain approximately +3.5 volts of reverse bias on the base of Q2, keeping it cut off. With Q2 cut off, resistors R3 and R6 will provide a path for Q1 base current, clamping Q1 in saturation. This condition is stable and will not be changed until an input is received on pin 3 or pin 6. Pin 6 is in "1" input, in that a positive pulse above 0 volts at pin 6 will cause CR3 to conduct, thus driving the base of Q1 positive above 0 volts, reverse biasing Q1, subsequently cutting Q1 off. As Q1 is cut off its collector will go negative and due to the resistor divider, R1 and R7, the base of Q2 will go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and due to the resistor divider of R2 and R3 the base of Q1 will be reverse biased at approximately +3.5 volts, keeping Q1 cut off, after the input pulse has passed. The network will remain in the "1" state until reset by a positive pulse on pin 7 or triggered from a pulse on pin 3, the counting input. If a positive pulse is applied on pin 3 through an external capacitor for differentiation, both Q1 and Q2 will be cut off. Capacitors C1 and C2 retain charges which are dependent upon which one of the transistors was saturated before the input pulse occurred. Since the input pulse is differentiated by a small input capacitor, it will last a very short time, less than one microsecond. At this point, the internal capacitors C1 and C2 take over, turning on the transistor that had previously been off. For example; assume the network is the "1" state, therefore Q1 is cut off and Q2 is saturated. The voltage across C1 will be approximately 3.5 volts and across C2 will be approximately 26 volts. When pin 3 goes positive above 0 volts, both bases will be driven positive, cutting the transistors off. The collector of Q2 starts to go negative from 0 volts to -23 volts. Since this occurs almost instantaneously and C1 has been charged only 3.5 volts the base of Q1 will go negative, turning Q1 on. As Q1 is turned on, Q2 is held cut off and we are now in the "0" state as explained previously. Note, since the collector of Q1 was at -23 volts before the pulse occurred on pin 3 and there wasn't any change of collector voltage when the pulse did occur. The base of Q2 would not experience any change through C2. The output pins of the network are 5 and 8. When the network is in the "0" state pin 5 will be at 0 volts and pin 8 will be approximately -23 volts and the reverse is true when the network is in the "1" state. Although the description of operation has been based on voltages of +15 volts and -25 volts this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.



Schematic,

TN90B Balanced Flip-Flop and Divider

Dwg. #A 103S90B

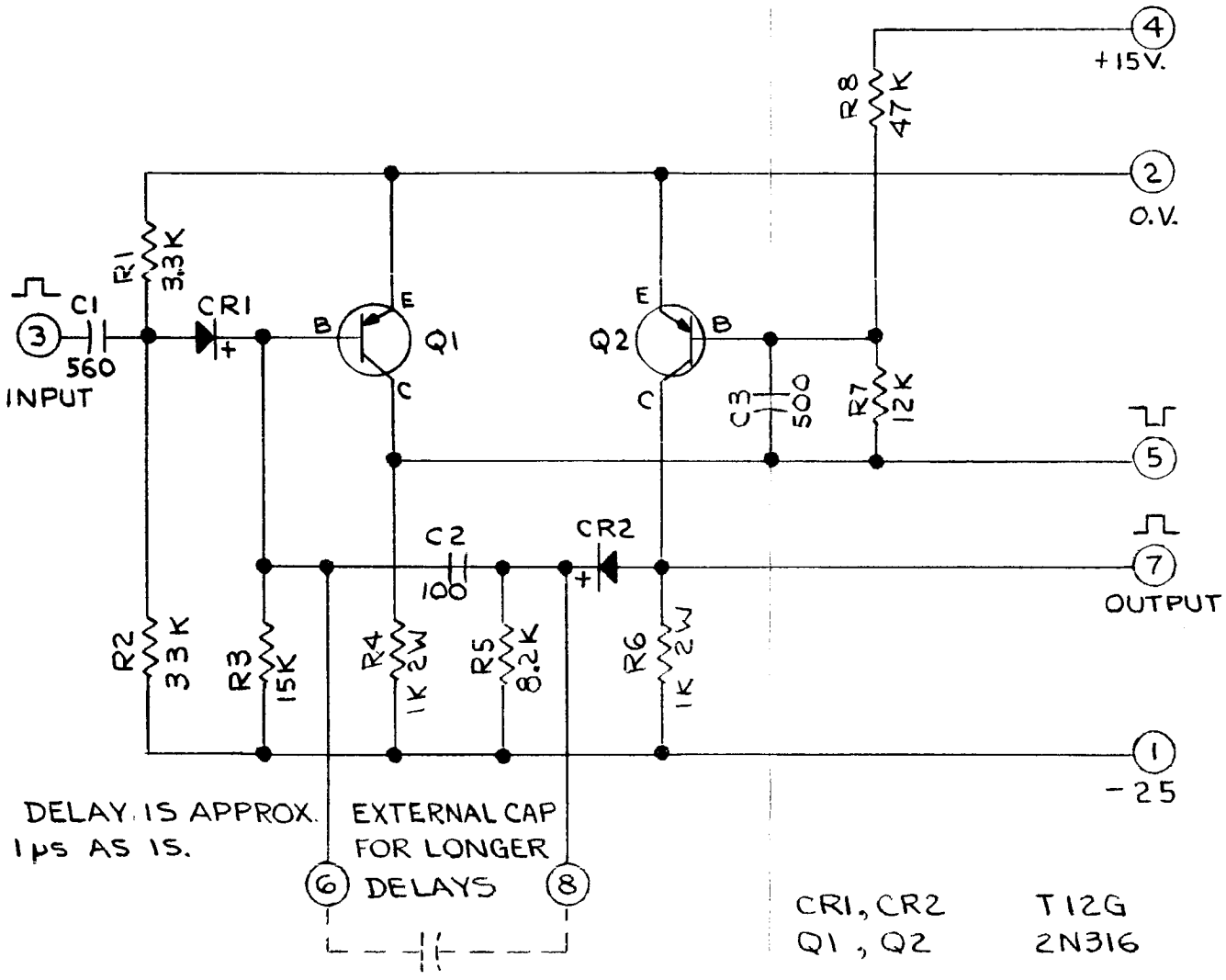
TN 111
ONE-SHOT (MONOSTABLE MULTIVIBRATOR)

The TN111 is a one-shot (monostable multivibrator) used for generating a pulse which can be varied from a minimum of one microsecond to well over 200 microseconds. In the quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage divider R7 and R8 is connected between +15 volts and zero volts, establishing a reverse bias voltage on the Q2 base and keeping Q2 cut off.

Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise will not trigger the network. A positive pulse of not less than 10 volts, with a rise time not greater than 0.5 microseconds, will trigger the network by cutting off transistor Q1. Transistor Q1 is cut off when the input pulse raises the base voltage of transistor Q1 above zero volts. Capacitor C1 is used to differentiate the input pulse so that a long duration input pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts to almost zero volts. This rise in voltage is coupled to the base of transistor Q1 through capacitor C2, keeping transistor Q1 at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return to less than zero volts. Q1 saturates again and cuts off Q2.

This time can be lengthened by adding capacitance in parallel with capacitor C2. The terminals of C2 are brought out on pins 6 and 8 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a dc path for the current of C2. This network will operate on lower power supply voltages, such as +12 and -20 volts, or +10 and -15 volts.



Schematic,

TN111 One-Shot Monostable Multivibrator

Dwg. #A103S111A

TN 130 B
CORE DRIVER

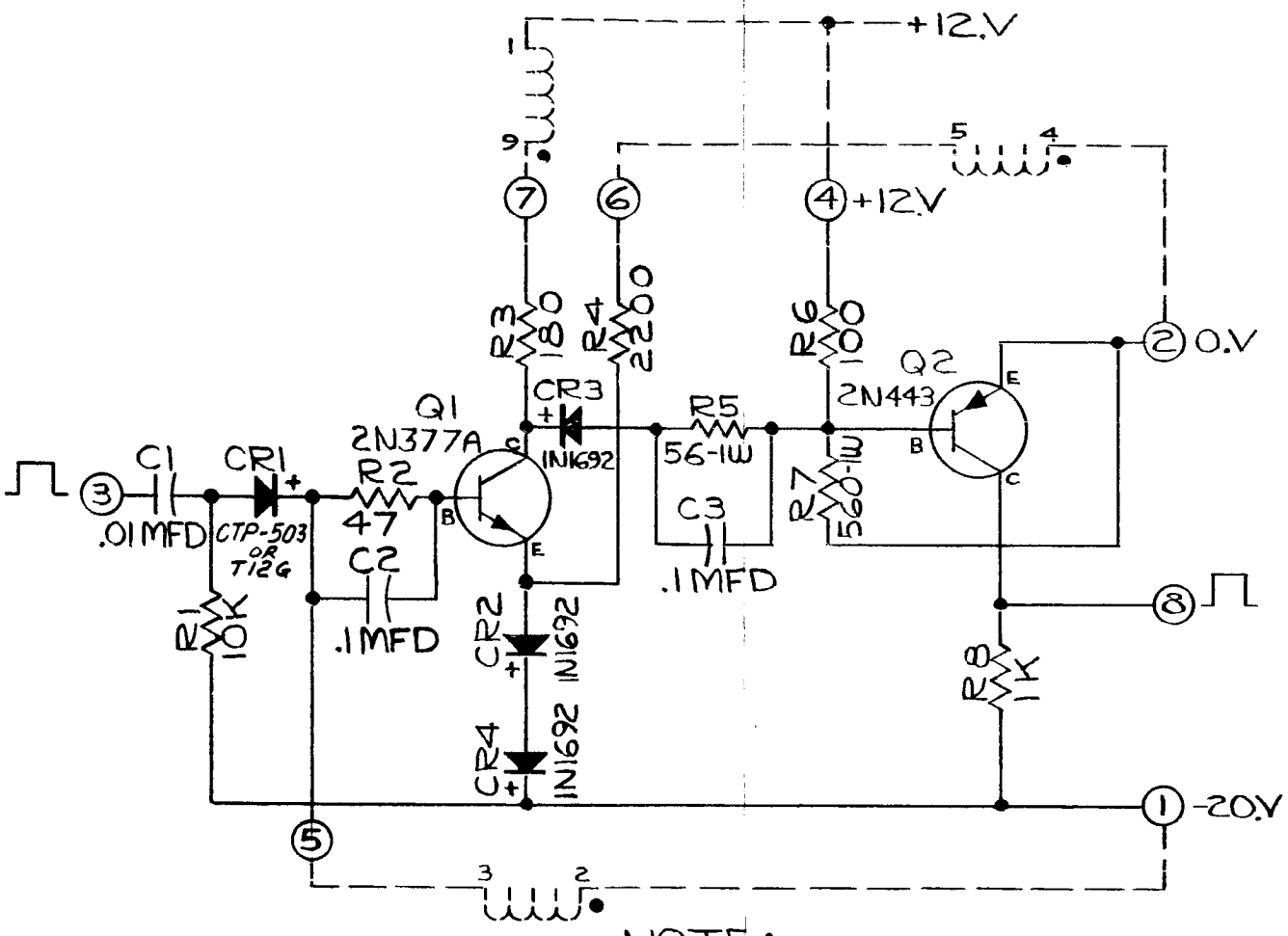
The TN130B is a blocking oscillator with amplifier which generates a positive going pulse from -20 volts to 0 volts, with a time duration determined by the core with which it is used. The TN130B is normally used with a MEC Model MN13 core, which gives it a pulse width of approximately 40 microseconds.

In the quiescent condition, transistor Q1 is maintained in cut off. The emitter voltage of Q1 is determined by the forward voltage drop of diodes CR2 and CR4 (1.5 volts) and is at approximately -18.5 volts. The base of Q1 is returned to -20 volts through R2 and the feedback winding of the core, connected from pin 5 to -20 volts. The d-c impedance of the feedback winding is approximately 5 ohms; thus the base of Q1 is nearly -20 volts, keeping Q1 reverse biased approximately 0.7 volts and properly cut off. Since there is no Q1 collector current, the collector voltage is +12 volts.

A positive going input pulse at pin 3 is coupled by capacitor C1, diode CR1, and capacitor C2, paralleled with R2 to the base of Q1. This pulse starts Q1 conducting. The resulting Q1 collector current passes through the collector winding of the external core. This generates a voltage across the collector winding coupled through the core to the feedback winding. By noting the phasing of the windings on the core, it can be seen that, as the collector voltage becomes negative, the voltage at pin 5 is becoming positive. This in turn drives Q1 further into conduction, even after the input pulse has been differentiated by C1. Q1 saturates in approximately one microsecond with an emitter-collector voltage of approximately 0.25 volts. Q1 will remain saturated as long as transformer action in the core continues to drive pin 5 of the TN network sufficiently positive to cause Q1 base current to flow. The pulse width (approximately 40 microseconds for an MN13 core) is determined by the characteristics of the core.

When the core material finally reaches saturation, transformer action in the core will cease, the feedback winding will no longer drive pin 5 positive, and Q1 base current will stop. This cuts off Q1. With no current in the collector winding of the core, the current in the reset winding resets the core. This reset current is furnished to the reset winding (pins 4 and 5 of the core) through resistor R4 and diodes CR2 and CR4. This involves going from the plus saturation condition attained during the output pulse to a minus saturation condition (reset). During this time, the voltages at the feedback winding and the collector winding are reversed. The reversal of a voltage at the feedback winding increases the reverse bias on Q1. The reversal of voltage in the collector winding tends to drive the output voltage somewhat more positive than the +12 volts on pin 7. It takes approximately 30 microseconds for the reset action to be accomplished.

The amplifier section Q2 is normally biased to cutoff by voltage divider R7 and R6. With no collector current flowing, the quiescent collector voltage of Q2 is -20 volts. The negative going pulse generated by the blocking oscillator section is coupled to the amplifier base through CR3, R5, and C3. The diode provides for rapid cut off of the amplifier, thereby minimizing the fall time. R5 and C3 serve as base current limiting and rise time determinants. The load is connected between -20 volts and 0 volts and should be limited to no less than 8 ohms (20 to 24 MN11 cores).



NOTE:
ALL RESISTORS ½ WATT ±10%
UNLESS OTHERWISE NOTED.

Schematic,

TN130B Core Driver

Dwg. #A103S130B

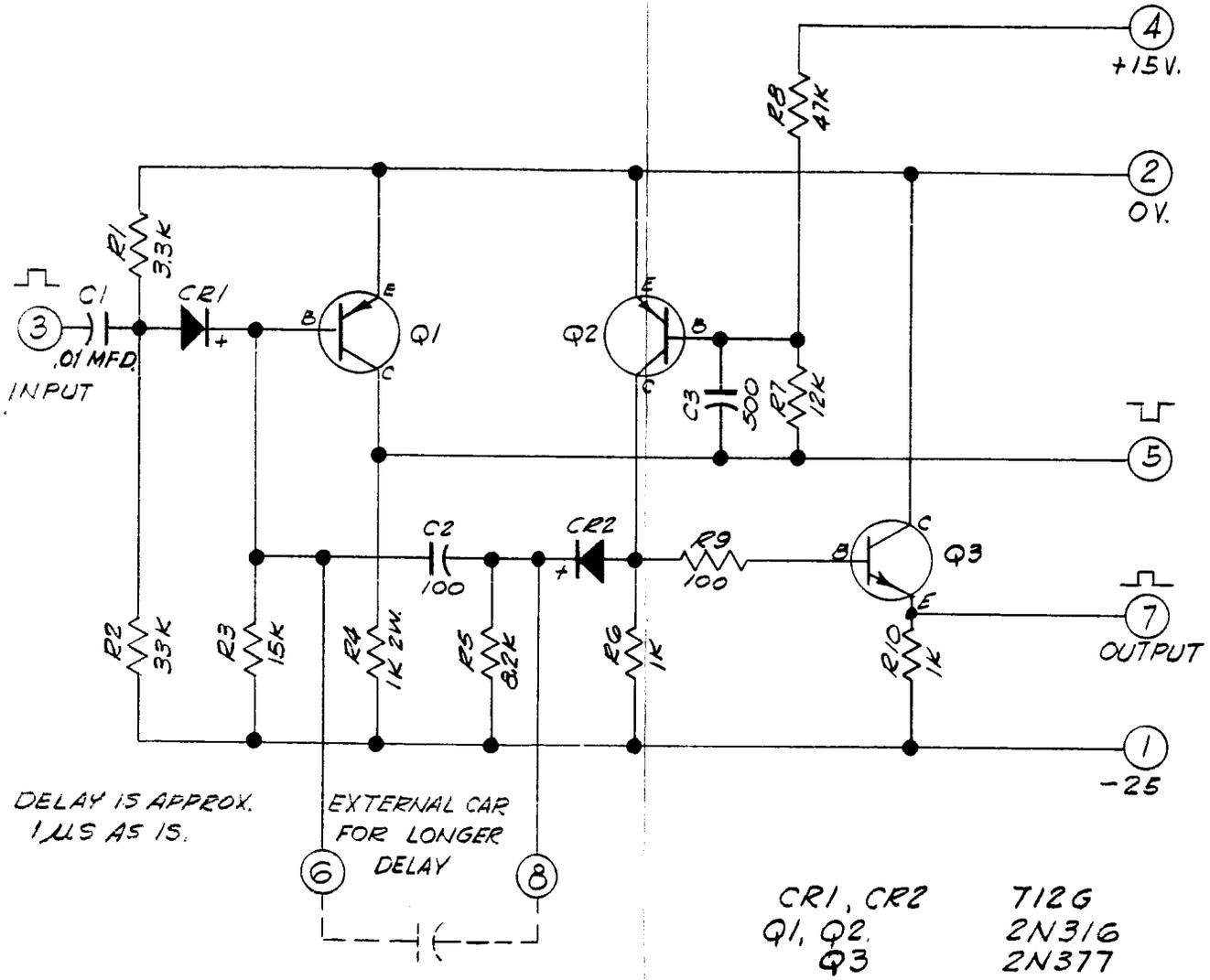
TN 138
ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN-138 is a monostable flip-flop used for generating a pulse which can be varied in width from a minimum of 2 microseconds to over 200 microseconds. In quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since Q1 is saturated, voltage divider resistors R7 and R8 are connected between +15 volts and 0 volts, establishing a positive bias voltage on the base of transistor Q2, and keeping Q2 cut off. Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise does not trigger the network.

A positive pulse of not less than 10 volts, with a rise time not greater than 1 microsecond, will trigger the network by cutting off Q1. Transistor Q1 is cut off when the input pulse raises the base voltage above 0 volts. Capacitor C1 is used to differentiate the input pulse so that a long duration pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of Q2, and Q2 saturates. The collector voltage of Q2 will rise from -25 volts to nearly 0 volts. This rise of voltage is coupled to the base of Q1 through capacitor C2, keeping Q1 at cut-off until the R-C time of C2 and resistor R3 allows the base voltage of Q1 to return to less than 0 volts. Transistor Q1 now saturates again and cuts off Q2. This time can be lengthened by adding capacitance in parallel with C2.

The terminals of C2 are brought out on pins 6 and 8 of the network. Diode CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through resistor R6. Resistor R5 provides a dc path for current of C2. Transistor Q3 is the emitter follower which will drive a load of 200 ohms.



Schematic,

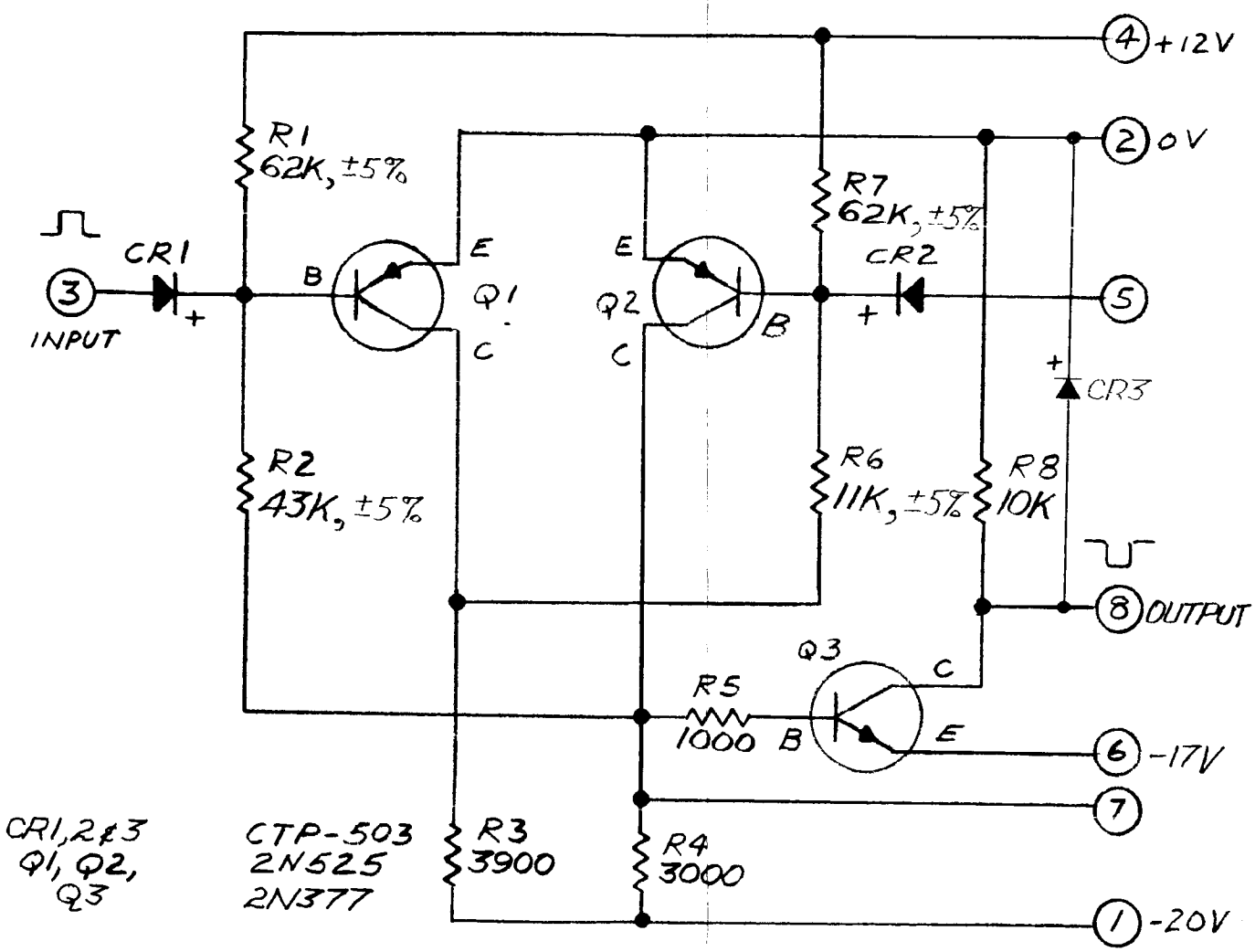
TN138 One-Shot with Emitter Follower Output

Dwg. #A103S138

TN 144
FLIP-FLOP WITH PULSE AMPLIFIER OUTPUT

A TN144 is a bistable flip-flop with a pulse amplifier output which can be used to drive a load of 85 ohms or more. Since most flip-flops are limited to the amount of loading, which affects the switching of the flip-flop, a pulse amplifier has been added to permit greater loads. A transistorized neon indicator may be connected in parallel with the load to indicate the states of the flip-flop. The network is normally defined as being in the "0" state when transistor Q1 is saturated and Q2 and Q3 are cut off. The "1" state is the condition when Q1 is cut off and Q2 and Q3 are saturated. Assuming that Q1 is saturated ("0" state), then its collector is at approximately -0.25 volt. Resistors R7 and R6 are then connected from +12 volts to 0 volts, and by divider action hold the base of Q2 at approximately +1.8 volts. Since the emitter of Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -0.5 volt, so the current through resistor R1 is approximately 0.2 milliamps. Since Q2 is cut off, its collector is at approximately -19 volts, and the current through R2 and R4 is therefore 0.4 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to clamp Q1 in saturation. This mode of operation is therefore stable. Q3 is cut off when Q2 is cut off, since the base of Q3 is at -19 volts, reverse biasing the emitter. Since Q3 is cut off, there is no collector current (except for leakage) and pin 8 is at approximately 0 volts. The input voltages at pins 3 and 5 must be somewhat negative during quiescent conditions. The flip-flop may be triggered to the "1" state by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, thus raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cuts off. With Q1 cut off, R7 and R6 are no longer connected between the +12 volts and 0 volts, and Q2 is no longer clamped off. Instead, base current of Q2 may now flow through resistors R6 and R3, cuasing Q2 to saturate. Now resistors R1 and R2 are connected from +12 volts to 0 volts, and clamp the base of Q1 at approximately +5 volts, holding Q1 in a cut off condition after the input pulse passes. As Q2 is saturated and its collector goes positive, the base of Q3 goes positive enough to allow Q3 to saturate. R5 limits the base current of Q3. As Q3 saturates, pin 8 (the output pin) goes negative to approximately -17 volts. R8 is the collector load resistor of Q3, to furnish a minimum collector current when there is no external load from pin 8 of the network to 0 volts. This is the other stable condition which will be maintained until Q2 is cut off by a positive pulse on pin 5. A positive pulse (normally called reset) on pin 5 will allow base current from Q1 to be conducted through R2 and R4, driving Q1 back into saturation and restoring the initial condition. Diode CR3 is included to suppress the inductive effects of an external relay coil (if used) connected across pins 8 and 2. As Q3 goes from saturation to cut off, the relay coil is de-energized. However, the inductance of the relay coil attempts to

maintain the current through it by driving the voltage at pin 8 much more positive than 0 volts. If this were allowed to happen, Q2 could be damaged by the excessive collector-emitter voltage. During most phases of the cycle, CR3 is reverse biased; consequently, it does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven positive by the relay inductance, CR3 is forward biased and conducts, providing a path for the current through the relay coil and eliminating the excessive transient voltage to appear on the collector of Q3.



Schematic,

TN144 Flip-Flop with Pulse Amplifier Output

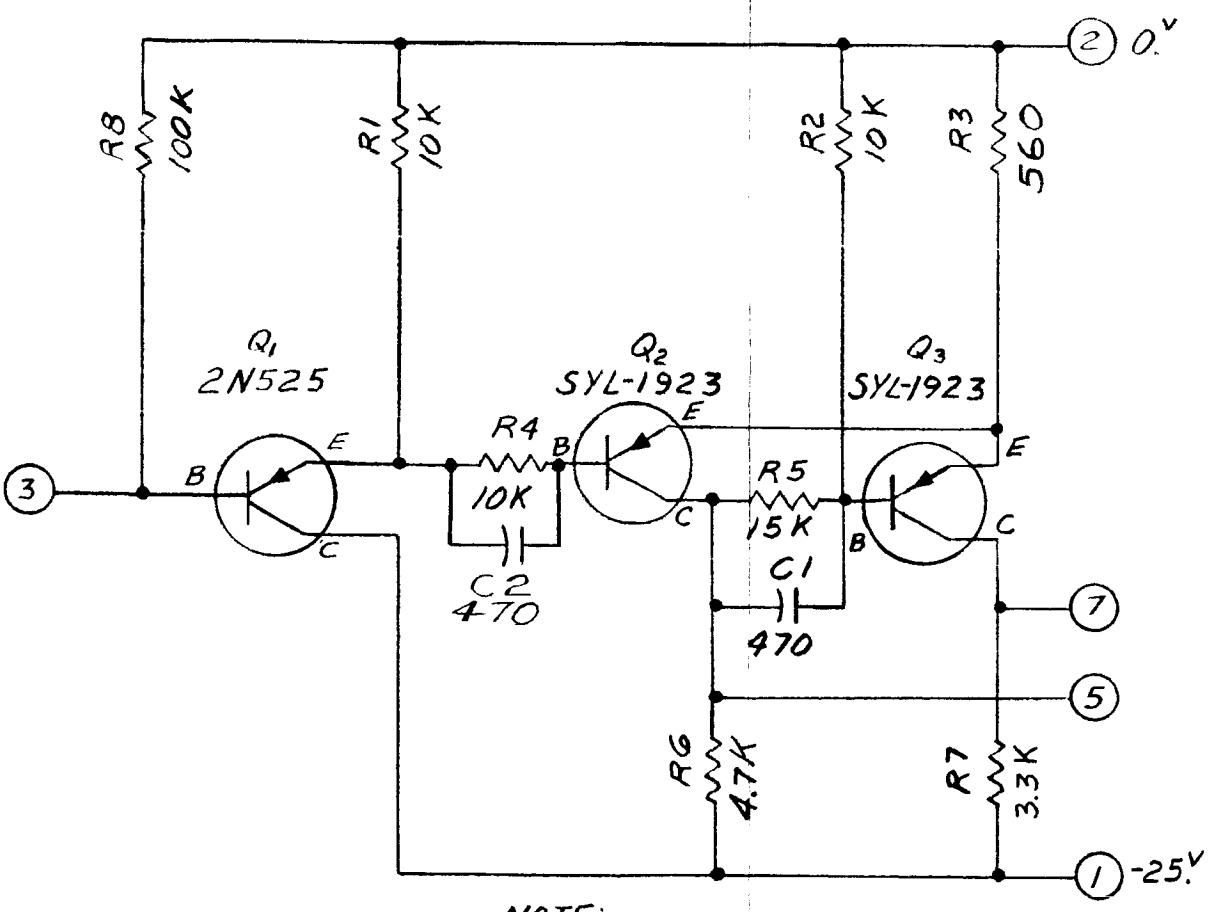
Dwg. #A103S144A

TN 150
SCHMITT TRIGGER

TN150 is a Schmitt trigger preceded by an emitter follower which presents an input impedance at approximately 70,000 ohms at pin 3. The circuit switches rapidly (in approximately 0.3 microseconds) from one state to the other with either a pulse or DC level change on pin 3 input. With the input disconnected or at a positive level, Q1 and Q2 are cut off and Q3 is conducting.

Q1 is cut off by R8 returning the base of Q1 to a more positive voltage than the emitter, and Q2 is cut off by R1 returning the base of Q2 to a more positive voltage than the emitter of Q2. The emitter of Q2 and Q3 are at a negative voltage $-E_2$ developed by the current flow through R3, Q3 and R7. Q3 is conducting because the base is forward biased by the resistor divider R2, R5 and R6, since Q2 is cut off. When the input, pin 3, is taken to a negative voltage, Q1 is turned on, which makes the emitter of Q1 go negative (-25 volts). This will forward bias Q2, causing it to conduct. When Q2 is conducting, the base voltage of Q3 is raised to a more positive value through the emitter voltage, thus reversing the bias on Q3 and cutting it off. This causes the collector voltage of Q3 to go from -25 volts to approximately -3 volts. C1 is used to speed up the switching time. The outputs, pin 7 and pin 5, are opposite polarity pulses from -25 volts to -3 volts. When the output is removed or goes positive, the circuit is returned to the original state.

Although the description of operation has been based on power supply voltages of -25 volts, this network will operate equally well on supply voltages down to -10 volts.



NOTE:
1. ALL RESISTORS $\frac{1}{2}$ WATT ±10% UNLESS OTHERWISE SPECIFIED.

Schematic,

TN150 Schmitt Trigger

Dwg. #A103S150A